SCHEME OF EXAMINATION

&

DETAILED SYALLBUS

for

MASTER OF TECHNOLOGY [INFORMATION TECHNOLOGY]
WEEKEND PROGRAMME

Offered by

University School of Information Technology

Guru Gobind Singh
Indraprastha University

Guru Gobind Singh Indraprastha University
Kashmere Gate, Delhi [INDIA] –110 006
www.ipu.ac.in

w.e.f. August 2005

Admission Criteria & Eligibility

Admission Criteria:

Admission will be based on the merit list of the candidates in the qualifying examination. Preference will be given to candidates of Category A. However, if there is any vacancy left then the seats will be offered to the candidates of Category B as per merit list of the candidates in the qualifying examinations.

Entry Level : 60% or equivalent in the qualifying examination.

Category A:
B.Tech./B.E. in Computer Science / Computer Science & Engineering / Computer Engineering / Information Technology or equivalent
MCA / MCA (Software Engineering) or equivalent three year programme
B.Tech. / B.E. in Electronics & Communication / Electronics Engineering or Equivalent
M.Sc. in IT / Computer Science, Information Science & Technology or equivalent
B.Tech. / B.E. in Electrical Engineering or Equivalent
M.Sc. in Electronics or equivalent

Category B:
B.Tech. / B.E. in any discipline or equivalent
M.Sc. in Physics/Mathematics/Statistics or equivalent

Experience:
In addition to above qualification(s), candidates should also have at least one year of professional/teaching experience after completing the qualifying examination as on 30th June.

Merit List:
Merit List will be prepared on the following basis:
Percentage of Qualifying degree
One Mark per additional year of experience up to maximum of **five**.

Note:
For CS background:
1. B.Tech. / B.E. in Computer Science/Computer Science & Engineering / Computer Engineering/Information Technology or equivalent.
MCA / MCA (Software Engineering) or equivalent three-year programme.
M.Sc. in IT / Computer Science, Information Science & Technology or equivalent

For Non-CS background
2. Other than above qualification

M.Tech. [Information Technology]
Weekend Programme

First Semester

Code No.	Paper	Credits	Contact Hrs./ Semester	Self Study Hours
ITW – 601	Operating Systems	3	40	15
ITW – 603	Digital System Design	3	40	15
ITW – 605	Programming & Data Structure **(For Non CS background)**	3	40	15
	Or			
ITW – 607	Communication System **(For CS background)**			
Practicals				
ITW – 651	Digital System Design Lab	2	60	40
ITW – 653	Programming & Data Structure Lab **(For Non CS background)**	2	60	40
	Or			
ITW – 655	Communication System Lab **(For CS background)**		60	40
ITW – 657	Term Paper - I*	2	-	30
	TOTAL	**15**		

* **Non University Exam System**

M.Tech. [Information Technology]
Weekend Programme

Second Semester

Code No.	Paper	Credits	Contact Hrs./ Semester	Self Study Hours
ITW – 602	Object Oriented Technology	3	40	15
ITW – 604	Algorithm Analysis & Design	3	40	15
ITW – 606	Foundation of Computer Science **(For non CS background)**	3	40	15
	Or			
ITW – 608	Data Communication **(For CS background)**		40	15
Practicals				
ITW – 652	Algorithm Analysis & Design Lab	2	60	40
ITW – 654	Object Oriented Technology Lab	2	60	40
ITW – 656	Foundation of Computer Science Lab **(For non CS background)**	2	60	40
	or			
ITW – 658	Data Communication Lab **(For CS background)**		60	40
ITW – 660	Term Paper – II*	2	-	30
	TOTAL	**17**		

*** Non University Exam System**

M.Tech. [Information Technology]
Weekend Programme

Third Semester

Code No.	Paper	Credits	Contact Hrs./ Semester	Self Study Hours
ITW – 701	Database Management System	3	40	15
ITW – 703	Advanced Computer Networks	3	40	15
ITW – 705	Computer Graphics	3	40	15
Practicals				
ITW – 751	Database Management System Lab	2	60	40
ITW – 753	Advanced Computer Networks Lab	2	60	40
ITW – 755	Computer Graphics Lab	2	60	40
ITW – 757	Term Paper – III*	2	-	30
	TOTAL	**17**		

*** Non University Exam System**

M.Tech. [Information Technology]
Weekend Programme

Fourth Semester

Code No.	Paper	Credits	Contact Hrs./ Semester	Self Study Hours
ITW – 702	Software Engineering	3	40	15
ITW – 704	Cellular & Mobile Communication	3	40	15
Elective I (choose any one)		3	40	15
ITW – 706	Multimedia Technology			
ITW – 708	VLSI Design			
ITW – 710	Real Time Systems & Software			
ITW – 712	Data Warehousing & Data Mining			
ITW – 714	AI & Expert System			
ITW – 716	Digital Signal Processing			
ITW – 718	Theory of Computation			
ITW – 720	Internet & Web Technology			
ITW – 722	Network Security			
ITW – 724	Advanced Computer Architecture			
ITW – 726	Robotic Engineering			
Practicals				
ITW – 752	Cellular & Mobile Communication Lab	2	60	40
ITW – 754	Software Engineering Lab	2	60	40
ITW – 756	Elective-I Lab	2	60	40
ITW – 758	Project work - I*	3	-	
	TOTAL	**18**		

***Non University Exam System**

M.Tech. [Information Technology]
Weekend Programme

Fifth Semester

Code No.	Paper	Credits	Contact Hrs./ Semester	Self Study Hours
ITW – 801	Software Testing	3	40	15
Elective II (choose any one)		3	40	15
ITW – 803	Neural Network			
ITW – 805	Embedded Systems Design			
ITW – 807	Fuzzy Logic			
ITW – 809	Digital Image Processing			
ITW – 811	Designing with ASICSs			
ITW – 813	Object Oriented Software Engineering			
ITW – 815	Cognitive Psychology			
ITW – 817	Requirement & Estimation Techniques			
ITW – 819	Digital VLSI Design			
ITW – 821	Telecommunication Networks			
Elective III (choose any one)		3	40	15
ITW – 823	Programming with AVR Microcontroller			
ITW – 825	Natural Language Processing & Understanding			
ITW – 827	Enterprise Resource Planning			
ITW – 829	Soft Computing			
ITW – 831	Software Quality Assurance & Certification			
ITW – 833	Network Programming			
ITW – 835	Advanced VLSI Design			
ITW - 837	Advanced Digital Circuit Design			
ITW – 839	Mobile Computing			
ITW – 841	Total Quality Management			
Practicals				
ITW – 851	Software Testing Lab	2	60	40
ITW – 853	Elective-II Lab	2	60	40
ITW – 855	Elective-III Lab	2	60	40
ITW – 857	Project Work – II*	4	-	
	TOTAL	**19**		

***Non University Exam System**

M.Tech. [Information Technology]
Weekend Programme

Sixth Semester

Code No.	Paper	Credits	Contact Hrs./ Semester
ITW – 802	Dissertation	15	-
ITW – 804*	Seminar & Progress Reports	03	-
ITW – 806*	Comprehensive Viva	02	-
	Total	**20**	

***Non University Exam System**

Note:

1. The total number of credits of the programme M.Tech. [Information Technology] = 106

2. Each student shall be required to appear for examinations in all courses. However, for the award of the degree a student shall be required to earn the minimum of 100 credits.

Note: Elective course(s) will be offered only if it is opted by 33% of actual strength of the class.

Paper Code: ITW – 601 **L T C**
Paper:Operating System **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction, What is an Operating System, Simple Batch Systems, Multiprogrammed Batches systems, Time-Sharing Systems, Personal-computer systems, Parallel systems, Distributed Systems, Real-Time Systems

Memory Management: Background, Logical versus Physical Address space, swapping, Contiguous allocation, Paging, Segmentation, Segmentation with Paging

Virtual Memory: Demand Paging, Page Replacement, Page-replacement Algorithms, Performance of Demand Paging, Allocation of Frames, Thrashing. **[No. of Hrs.: 10]**

UNIT – II

Processes: Process Concept, Process Scheduling, Operation on Processes, Cooperating Processes, Interprocess Communication

CPU Scheduling: Basic Concepts, Scheduling Criteria, Scheduling Algorithms, Multiple-Processor Scheduling, Real-Time Scheduling, Algorithm Evaluation

Process Synchronization: Background, The Critical-Section Problem, Synchronization Hardware, Semaphores, Classical Problems of Synchronization, Critical Regions, Monitors.

[No. of Hrs.: 10]

UNIT – III

Deadlocks: System Model, Deadlock Characterization, Methods for Handling Deadlocks, Deadlock Prevention, Deadlock Avoidance, Deadlock Detection, Recovery from Deadlock, Combined Approach to Deadlock Handling.

Device Management: Techniques for Device Management, Dedicated Devices, Shared Devices, Virtual Devices; Device Characteristics-Hardware Consideration, Input or Output Devices, Storage Devices, Channels and Control Units, Independent Device Operation, Buffering, Multiple Paths, Block Multiplexing, Device Allocation Consideration,

Secondary-Storage Structure: Disk Structure, Disk Scheduling, Disk Management, Swap-Space Management, Disk Reliability, Stable-Storage Implementation **[No. of Hrs.: 10]**

UNIT – IV

Information Management: Introduction, A Simple File System, General Model of a File System, Symbolic File System, Basic File System, Access Control Verification, Logical File System, Physical File System File-System Interface: File Concept, Access Methods, Directory Structure, Protection, Consistency Semantics File-System Implementation: File-System Structure, Allocation Methods, Free-Space Management, Directory Implementation **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Silbersachatz and Galvin, "Operating System Concepts", Pearson, 5th Ed., 2001
2. Madnick E., Donovan J., "Operating Systems", Tata McGraw Hill, 2001

REFERENCES:

1. Tannenbaum, "Operating Systems", PHI, 4th Edition, 2000

Paper Code: ITW – 603 **L T C**
Paper: Digital System Design **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Specification of combinational systems using VHDL, Introduction to VHDL, Basic language element of VHDL, Behavioral Modeling, Data flow modeling, Structural modeling, Subprograms and overloading, VHDL description of gates. **[No. of Hrs.: 10]**

UNIT – II

Description and design of sequential circuits using VHDL, Standard combinational modules, Design of a Serial Adder with Accumulator, State Graph for Control Network, design of a Binary Multiplier, Multiplication of a Signed Binary Number, Design of a Binary Divider. **[No. of Hrs.: 10]**

UNIT – III

Register- transfer level systems, Execution Graph, Organization of System, Implementation of RTL Systems, Analysis of RTL Systems, Design of RTL Systems. Data Subsystems, Storage Modules, Functional Modules, Data paths, Control Subsystems. **[No. of Hrs.: 10]**

UNIT – IV

Micro programmed Controller, Structure of a micro programmed controller, Micro instruction Format, Micro instruction sequencing, Micro instruction Timing, Basic component of a micro system, memory subsystem.

Overview of PAL, PLA, FPGA, CPLD **[No. of Hrs.: 10]**

TEXT BOOKS:

1. J. Bhaskar, " A VHDL Primer", Addison Wesley, 1999.
2. M. Ercegovac, T. Lang and L.J. Moreno, "Introduction to Digital Systems", Wiley,2000
3. C. H. Roth, "Digital System Design using VHDL", Jaico Publishing, 2001

REFERENCES:

1. VHDL Programming by Examples by Douglas L. Perry, TMH, 2000
2. Hardware Description Languages by Sumit Ghose, PHI, 2000
3. The Designer Guide to VHDL by P.J. Ashendern; Morgan Kaufmann Pub. 2000
4. Digital System Design with VHDL by Mark Zwolinski; Prentice Hall Pub. 1999
5. Designing with FPGA & CPLDs by Zeidman; CMP Pub. 1999
6. HDL Chip Design by Douglas J. Smith; Doone Pub. 2001

Paper Code:ITW-605 **L T C**
Paper: Programming and Data Structures **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

C program structures, Variables, Data Types, Declarations, Operators (Arithmetic, Relational, Logical), increment and decrement operators, Assignment operators and expressions, Arithmetic expressions, statements, symbolic constants, conditional expressions, Bitwise operators, precedence and order of evaluations, input-output functions.

Statements and Blocks, branching statements (if, switch), Loops (while, for, do-while, repeat-until), Break and continue, go to and labels.

Functions, external variables, scope rules, header files, static variables, initialization, parameter passing (call-by-value, call-by-reference), recursion, C preprocessor. **[No. of Hrs.: 10]**

UNIT – II

Pointers and addresses, pointers and function arguments, pointer and arrays, address arithmetic, character pointers and functions, pointer arrays, multidimensional arrays, initialization of pointer arrays, pointers and multidimensional arrays, command line arguments, memory management.

Structures: Defining and processing, passing to a function, Unions.

Files: Standard input and output, formatted output, formatted input, file access, miscellaneous functions. **[No. of Hrs.: 10]**

UNIT – III

Data Structures: Arrays : representation and basic operations.

Linked list : Singly, Doubly, Circular and Doubly circular, definition, representation and their basic operations.

Stacks and queues : insertion, deletion. **[No. of Hrs.: 10]**

UNIT – IV

Trees : insertion, deletion, traversal (inorder, preorder and postorder), binary trees, AVL trees, B-trees, B+-trees. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Gottfried, "Schaum's Outline series in C Programming", McGraw Hill. 2003
2. Horowitz, E. and Sahni, S., "Fundamentals of Data Structures", Galgotia Publications. 2002

REFERENCES:

1. Kernighan and Ritche, "The C programming Language", PHI. 1999
2. Lipschultz, "Schaum's Outline series in Data Structures", McGraw Hill. 2001
3. Hutchison, R., "Programming in C", McGraw Hill. 1999
4. Johnsonbaugh, R. and Kalin M., "Applications programming in C", PHI. 2000
5. Rajaraman, V., "Computer programming in C", PHI. 2003

Paper Code:ITW 607 **L T C**
Paper: Communication System **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Analog Modulation:

Amplitude Modulation

Generation & Demodulation of AM waves, DSBSC waves, Coherent Detection of DSBSC Signal, Quardrature-Carrier Multiplexing, Generation of SSB waves, Demodulation of SSB waves.

[No. of Hrs.: 10]

UNIT – II

Angle Modulation:

Frequency & Phase Modulation, narrow & Wide-Band FM, BW of FM waves, Generation & Demodulation of FM waves, S/N ratio, Comparison of AM, FM & PM . **[No. of Hrs.: 10]**

UNIT – III

Pulse Analog Modulation:

Sampling theorem, Sampling of Low Pass and band pass signals, Aliasing, Aperture effect, PAM, PWM and PPM generation and demodulation, TDM, Cross talk, Spectral Analysis of PAM, PWM and PPM Waves, S/N ratio for different pulse modulation. **[No. of Hrs.: 10]**

UNIT – IV

Pulse – Digital Modulation:

Pulse Code Modulation signal to quantization noise ratio, Companding, probability of error for PCM in AWGN Channel, DPCM, DM and ADM modulators and demodulators, line coding, Inter symbol Interference.

Introduction to Information Theory:

Measurement of Information, Mutual Information Shannon's Theorem Source Coding, Channel Coding and Channel Capacity Theorem. Hauffman Code, Lempel – ziv code. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Tomasi, "Electronic Communications Systems", 4th Ed, Pearson Education. 2001
2. Taub & Schilling, "Principles of Communication Sytems", TMH. 2001

REFERENCES:

1. Hancock J. C., "An Introduction to the Principles of Communication Theory", TMH, 2002.
2. B. P. Lathi, "Communications Systems", 2000
3. Simon Haykins, "Communication Systems", John Wiley. 2002
4. S. Haykin, "Digital Communication", "Analog and Digital Communication", Wiley. 2002

ITW-651: Digital System Design Lab.
The practical will be based on Digital System Design.

Or

ITW-653: Programming and Data Structures Lab.
The practical will be based on Programming and Data Structures.

ITW-655: Communication Systems Lab.
The practical will be based on Communication Systems.

ITW - 657* Term paper – I

Objective: Students are required select a topic of current research/development and prepare a report on it.

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format (available on www.ipu.ac.in). The student will have to present the progress of the work through seminars. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

*** Non University Exam Scheme**

Paper Code:ITW- 602 **L T C**
Paper: Object Oriented Technology **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction: Introducing Object Oriented Approach, Relating to other paradigms(functional, data decomposition)

Basic terms and ideas: Abstration, Encapsulation, Inheritance, Polymorphism, Review of C, Difference between C and C++ - cin, cout, new, delete operators. **[No. of Hrs.: 10]**

UNIT – I I

Classes and Objects: Encapsulation, information hiding, abstract data types, object & classes, attributes, methods. C++ class declaration, state identity and behavior of an object, constructors and destructors, instantiation of objects, default parameter value, object types, C++ garbage collection, dynamic memory allocation, metaclass/abstract classes. **[No. of Hrs.: 10]**

UNIT – I II

Inheritance, Class hierarchy, derivation – public, private & protected; aggregation, composition vs classification hierarchies, polymorphism, operator overloading, generic function – template function, function name overloading, overriding inheritance methods, run time polymorphism, function name overloading, Overriding inheritance methods, Run time polymorphism, Multiple Inheritance.

[No. of Hrs.: 10]

UNIT – I V

Files and Exception Handling: Persistent objects, Streams and files, Namespaces, Exception handling, Generic Classes, Generic Functions.

Standard Template Library: Standard Template Library, Overview of Standard Template Library, Containders, Algorithms, Iterators, Other STL Elements, The Container Classes.

Standard Namespaces, Standard template libraries, Files & Streams, Stream Manipulators, Exception Handling. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. S. B. Lippman & J. Lajoie, "C++ Primer", 3rd Edition, Addison Wesley, 2000.
2. R. Lafore, "Object Oriented Programming using C++", Galgotia. 2003

REFERENCES:

1. E.Balaguruswamy, "Objected Oriented Programming with C++", TMH, 2003
2. A.R.Venugopal, Rajkumar, T. Ravishanker "Mastering C++", TMH, 2002
3. D . Parasons, "Object Oriented Programming with C++",BPB Publication. 2002
4. Steven C. Lawlor, "The Art of Programming Computer Science with C++", Vikas Publication. 2003

Paper Code:ITW-604	**L**	**T**	**C**
Paper: Algorithm Analysis and Design	**3**	**0**	**3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Preliminaries:

Review of growth of functions, Recurrences: The substitution method, The iteration method, The master method, Data Structures for Disjoint Sets.

Divide and Conquer Approach:

Merge Sort, Quick sort, Medians and Order statistics, Strassen's algorithm for Matrix Multiplications. **[No. of Hrs.: 10]**

UNIT – II

Dynamic Programming:

Elements of Dynamic Programming, Matrix Chain Multiplication, Longest common subsequence and optimal binary search trees problems.

Greedy Algorithms:

Elements of Greedy strategy, An activity selection problem, Huffman Codes, A task scheduling problem. **[No. of Hrs.: 10]**

UNIT – III

Graph Algorithms:

Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Strongly Connected Components, Algorithm for Kruskal's and Prim's for finding Minimum cost Spanning Trees, Dijkstra's and Bellman Fort Algorithm for finding Single source shortest paths. All pair shortest paths and matrix multiplication, Floyd – Warshall algorithm for all pair shortest paths.

[No. of Hrs.: 10]

UNIT – I V

String matching:

The naïve String Matching algorithm, The Rabin-Karp Algorithm, String Matching with finite automata, The Knuth-Morris Pratt algorithm.

NP-Complete Problem:

Polynomial-time verification, NP-Completeness and Reducibility, NP-Completeness Proof, NP-Complete problems. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. T. H. Cormen, C. E. Leiserson, R.L. Rivest, C. Stein, "Introduction to Algorithms", 2nd Edition, PHI. 2002

REFERENCES:

1. A.V. Aho, J. E. Hopcroft, J.D. Ulman, "The Design & Analysis of Computer Algorithms", Addison Wesley. 2000
2. V. Manber, "Introduction to Algorithms – A Creative Approach", Addison Wesley. 1999
3. Ellis Harwitz and Sartaz Sahani, "Fundamentals of Computer Algorithms", Galgotia. 2001

Paper Code:ITW – 606 **L T C**

Paper: Foundation of Computer Science **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Formal Logic: Statement, Symbolic Representation and Tautologies, Quantifiers, Predicator and validity, Normal form. Propositional Logic, Predicate Logic, Logic Programming and Proof of correctness. **[No. of Hrs.: 10]**

UNIT – II

Proof, Relation and Analysis of Algorithm: Techniques for theorem proving: Direct Proof, Proof by Contra position, Proof by exhausting cares and proof by contradiction, principle of mathematical induction, principle of complete induction. Recursive definitions, solution methods for linear, first-order recurrence relations with constant coefficients, Analysis of Algorithms involving recurrence relations-recursive binary search, quick sort, solution method for a divide-and-conquer recurrence relation.

Sets and Combinations: Sets, Subtracts, powersets, binary and unary operations on a set, set operations/set identities, fundamental country principles, principle of inclusion, exclusion and pigeonhole principle, permutation and combination, pascal's triangles, binominal theorem, representation of discrete structures. **[No. of Hrs.: 10]**

UNIT – III

Relation/function and matrices: Rotation, properties of binary rotation, operation on binary rotation, closures, partial ordering, equivalence relation, Function properties of function, composition of function, inverse, binary and n-ary operations, characteristics for, Permutation function, composition of cycles, Boolean matrices, Boolean matrices multiplication.

Lattices & Boolean Algebra: Lattices: definition, sublattices, direct product, homomorphism Boolean algebra: definition, properties, isomorphic structures (in particulars, structures with binary operations) subalgebra, direct product and homo-morphism, Boolean function, Boolean expression, representation & minimization of Boolean function. **[No. of Hrs.: 10]**

UNIT – IV

Graph Theory: Terminology, isomorphic graphs, Euler's formula (proof) four color problem (without proof) and the chromatic number of a graph, five color theorem. Trees terminology, directed graphs, Computer representation of graphs, Warshall's, algorithms, Decision Trees, Euler path & hamiltonian circuits, Shortest path & minimal spanning trees, Depth-first and breadth first searches, trees associated with DFS & BFS). Connected components, in order, preorder & post order trees traversal algorithms. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. J.P. Tremblay & R. Mamohan, "Discrete Mathematical Structure with Application to Computer Science," TMH, New Delhi (2000).
2. Kolman, Busby & Ross "Discrete Mathematical Structures", PHI,2004
3. Iyengar, Chandrasekaran and Venkatesh, "Discrete Mathematics", Vikas Publication,2004.

REFERENCES:

1. J. Truss, "Discrete Mathematics", Addison Wesley,2000
2. C.L.Liu, "Elements of Discrete Mathematics", McGraw Hill Book Company,2002.
3. M.Lipson & Lipshutz, "Discrete Mathematics", Schaum's Outline series,2000.

Paper Code:ITW–608 **L T C**
Paper: Data Communications **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Data Communications fundamentals: Communication model, computer communications architecture, OSI model, standards, analog and digital transmission, transmission media, line configuration, topologies, data communications codes, error detection and correlation methods.

[No. of Hrs.: 10]

UNIT – I I

Data Modem & Modulation: Data encoding methods, analog to digital, digital to analog etc., data modulation methods: ASK, FSK, PSK, QAM, M-ary systems, Modulation and coding trade-offs.

[No. of Hrs.: 10]

UNIT – I II

Data Communication methods: Data communication interface, line control unit, UART, USRT, Serial interface, terminal types.

Data link control & multiplexing: Flow control, error detection & control, IBM Bisync protocol, SDLC, HDLC, HDLC line procedures, time division multiplexing (TDM), FDM, carriers.

[No. of Hrs.: 10]

UNIT – I V

Data communication networking: Switched networks, circuit switching, packet switching, broadcast networks, LAN, WAN topologies, ATM & Frame relay, cell relay. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. William Stallings, "Data & Computer Communications", 6th Edition, PHI,2000.
2. Forouzan, "Data Communication & Networking", 2nd Edition, McGraw Hill,2003.

REFERENCES:

1. W. Tomasi, "Advanced Electronic Communication Systems", 2000
2. James Martin, "Telecommunications & The Computer", 3rd Edition, PHI. 2001
3. P. C. Gupta, "Data Communications, PHI, 2001.

ITW-652: Algorithm analysis and Design
The practical will be based on Algorithm analysis and Design.

ITW-654: Object Oriented Technology Lab
The practical will be based on Object Oriented Technology.

ITW-656: Foundation of Computer Sciences Lab
The practical will be based on Foundation of Computer Sciences.

Or

ITW-658: Data Communication Lab.
The practicals will be based on Data Communication Lab.

ITW – 656* Term Paper - II
Objective: Students are required select a topic of current research/development and prepare a report on it.

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format (available on www.ipu.ac.in). The student will have to present the progress of the work through seminars. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

*** Non University Exam Scheme**

Paper Code:ITW-701 **L T C**
Paper: Database Management Systems **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Basic Concepts and Conceptual Database Design: Database administrator & Database Users, Characteristics of the Database, Database Systems, Concepts and Architecture, Data Models, Schemes & Instances, DBMS Architecture & Data Independence, Database Languages & Interfaces, Overview of Hierarchical, Network & Relational Data Base Management Systems, Data Modelling Using The Entity-Relationship Model – Entities, Attributes and Relationships, Cardinality of Relationships, Strong and Weak Entity Sets, Generalization, Specialization, and Aggregation, Translating your ER Model into Relational Model

[No. of Hrs.: 10]

UNIT – II

Relational Model, Languages & Systems: Relational Data Model & Relational Algebra, Relational Model Concepts, Relational Model Constraints, Relational Algebra, SQL – A Relational Database Language, Data Definition in SQL, View and Queries in SQL, Specifying Constraints and Indexes in SQL, Practicing SQL commands using ORACLE.

[No. of Hrs.: 10]

UNIT – III

Relational Data Base Design and Oracle Architecture: Functional Dependencies & Normalization for Relational Databases, Functional Dependencies, Normal Forms Based on Primary Keys, (1NF, 2NF, 3NF & BCNF), Lossless Join and Dependency Preserving Decomposition, Oracle 8 Architecture, Database Storage, Oracle Software Structures, Shared Database Access Mechanism, Database Protection. **[No. of Hrs.: 10]**

UNIT – IV

Transaction Management: Transaction Concept and State, Implementation of Atomicity and Durability, Concurrent Executions, Serializability, Recoverability, Implementation of Isolation, Concurrency Control Techniques, Lock-Based Protocols, Timestamp-based Protocols, Validation – based Protocols, Multiple Granularity, Multiversion Schemes, Deadlock Handling, Recovery System, Failure Classification, Storage Structure, Recovery and Atomicity, Log-based Recovery, Shadow Paging. Concepts of Object Oriented Database Management Systems, Distributed Data Base Management Systems.

[No. of Hrs.: 10]

TEXT BOOKS:

1. Korth, Silberschatz, "Database System Concepts", 4th Ed., TMH, 2000.
2. Steve Bobrowski, "Oracle 8 Architecture", TMH, 2000

REFERENCES:

1. Date C. J., "An Introduction to Database Systems", 7th Ed., Narosa Publishing, 2004
2. Elmsari and Navathe, "Fundamentals of Database Systmes", 4th Ed., A. Wesley, 2004
3. Ullman J. D., "Principles of Database Systems", 2nd Ed., Galgotia Publications, 1999.

Paper Code:ITW –703 **L T C**
Paper:Advanced Computer Networks **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Review of Physical, Layer, Data link layer, LAN Technologies, ISDN, Frame-relay & ATM, Datalink Protocol. **[No. of Hrs.: 10]**

UNIT – II

Network Layer: ARP, RARP, ICMP, Routing Algorithms and Protocols, Router Operation, Router Configuration, Internetworking, IPv4 Protocol, IPv6 (an overview).

[No. of Hrs.: 10]

UNIT – III

User Datagram Protocol: Header, Checksum and Port Numbers.

Transmission Control Protocol: Services and Headers, Connection establishment and Termination, Timeout of Connection Establishment and TCP timeout and retransmission, Maximum Segment Size, Reset Segments, TCP Options. **[No. of Hrs.: 10]**

UNIT – IV

Application Layer: DNS, SNMP, RMON, Electronic Mail, WWW.

Network Security: Firewalls (Application and packet filtering), Virtual Private Network, Cryptography **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Behrouz A. Forouzan, "TCP/IP Protocol Suit", TMH, 2000.
2. Tananbaum A. S., "Computer Networks", 3rd Ed., PHI, 1999.

REFERENCES:

1. Black U, "Computer Networks-Protocols, Standards and Interfaces", PHI, 1996.
2. Stallings W., "Data and Computer Communications", 6th Ed., PHI, 2002.
3. Stallings W., "SNMP, SNMPv2, SNMPv3, RMON 1 & 2", 3rd Ed., Addison Wesley, 1999.
3. Laurra Chappell (Ed), "Introduction to Cisco Router Configuration", Techmedia, 1999.

Paper Code:ITW – 705 **L T C**
Paper: Computer Graphics **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Basic raster graphics algorithms for drawing 2 D Primitives liner, circles, ellipses, arcs, clipping, clipping circles, ellipses & polygon. **[No. of Hrs.: 10]**

UNIT – II

Polygon Meshes in 3D, curves, cubic & surfaces, Solid modeling.Geometric Transformation: 2D, 3D transformations, window to viewport transformations, acromatic and color models.

Graphics Hardware: Hardcopy & display techniques, Input devices, image scanners

[No. of Hrs.: 10]

UNIT – III

Shading Tech: Transparency, Shadows, Object reflection, Gouraud & Phong shading techniques. Visible surface determination techniques for visible line determination, Z-buffer algorithm, scanline algorithm, visible surfaces ray-tracing , recursive ray tracing, radio-city methods.

[No. of Hrs.: 10]

UNIT – IV

Procedural models, fractals, grammar-based models, multi-particle system, volume rendering.

[No. of Hrs.: 10]

TEXT BOOKS:

1. Foley et. al., "Computer Graphics Principles & practice", 2nd ed. AWL.,2000.

REFERENCES:

1. R.H. Bartels, J.C. Beatty and B.A. Barsky, "An Introduction to Splines for use in Computer Graphics and Geometric Modeling", Morgan Kaufmann Publishers Inc., 1987.
2. D. Hearn and P. Baker, "Computer Graphics", Prentice Hall, 1986.
3. C.E. Leiserson, T.H. Cormen and R.L. Rivest, "Introduction to Algorithms", McGraw-Hill Book Company, 1990.
4. W. Newman and R. Sproul, "Principles of Interactive Computer Graphics, McGraw-Hill, 1973.
5. R. Plastock and G. Kalley, "Theory and Problems of Computer Graphics", Schaum's Series, McGraw Hill, 1986.
6. F.P. Preparata and M.I. Shamos, "Computational Geometry: An Introduction", Springer-Verlag New York Inc., 1985.
7. D. Rogers and J. Adams, "Mathematical Elements for Computer Graphics", MacGraw-Hill International Edition, 1989
8. David F. Rogers, "Procedural Elements for Computer Graphics", McGraw Hill Book Company, 1985.
9. Alan Watt and Mark Watt, "Advanced Animation and Rendering Techniques", Addison-Wesley, 1992.

ITW-751: DBMS Lab
The practical will be based on Database Management System.

ITW-753: ACN Lab
The practical will be based on Advanced Computer Networks.

ITW-755: Computer Graphics Lab.
The practical will be based on Computer Graphics.

ITW – 757* Term Paper – III
Objective: Students are required select a topic of current research/development and prepare a report on it.

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format (available on www.ipu.ac.in). The student will have to present the progress of the work through seminars. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

*** Non University Exam Scheme**

Paper Code:ITW - 702 **L T C**
Paper: Software Engineering **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction: Software Crisis, Software Processes & Characteristics, Software life cycle models, Waterfall, Prototype, Evolutionary and Spiral Models

Software Requirements analysis & specifications: Requirement engineering, requirement elicitation techniques like FAST, QFD & Use case approach, requirements analysis using DFD, Data dictionaries & ER Diagrams, Rquirements documentation, Nature of SRS, Characteristics & organization of SRS. **[No. of Hrs.: 10]**

UNIT – II

Software Project Planning: Size Estimation like lines of Code & Function Count, Cost Estimation Models, Static single & Multivariable Models, COCOMO-II, Putnam resource allocation model, Risk Management.

Software Design: Cohesion & Coupling, Classification of Cohesiveness & Coupling, Function Oriented Design, Object Oriented Design, User Interface Design. **[No. of Hrs.: 10]**

UNIT – III

Software Metrics: Software measurements: What & Why, Token Count, Halstead Software Science Measures, Design Metrics, Data Structure Metrics, Information Flow Metrics.

Software Reliability: Importance, Hardware Reliability & Software Reliability, Failure and Faults, Reliability Models, Basic Model, Logarithmic Poisson Model, Software Quality Models,CMM & ISO 9001 **[No. of Hrs.: 10]**

UNIT – IV

Software Testing: Testing process, Design of test cases, functional testing: Boundary value analysis, Equivalence class testing, Decision table testing, Cause effect graphing, Structural testing, Path Testing, Data flow and mutation testing, Unit Testing, Integration and System Testing, Debugging, Alpha & Beta Testing, Regression Testing, Testing Tools & Standards.

Software Maintenance: Management of Maintenance, Maintenance Process, Maintenance Models, Reverse Engineering, Software Re-engineering, Configuration Management, Documentation.

[No. of Hrs.: 10]

TEXT BOOKS:

1. K. K. Aggarwal & Yogesh Singh, "Software Engineering", 2nd Ed, New Age International, 2005.
2. R. S. Pressman, "Software Engineering – A practitioner's approach", 5th Ed., McGraw Hill Int. Ed., 2001.

REFERENCES:

1. R. Fairley, "Software Engineering Concepts", Tata McGraw Hill, 1997.
2. P. Jalote, "An Integrated approach to Software Engineering", Narosa, 1991.
3. Stephen R. Schach, "Classical & Object Oriented Software Engineering", IRWIN, 1996.
4. James Peter, W. Pedrycz, "Software Engineering", John Wiley & Sons.
5. I. Sommerville, "Software Engineering", Addison Wesley, 1999.

Paper Code:ITW – 704 **L T C**
Paper: Cellular & Mobile Communication **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction to Cellular Mobile Systems

A basic cellular system, performance criteria, uniqueness of mobile radio environment, operation of cellular systems, planning a cellular system, overview of generations of cellular systems.

Elements of cellular radio systems Design and interference

General description of the problem, concept of frequency reuse channels, co-channel interference reduction factor, desired C/I from a normal case in an omni directional antenna system, cell splitting, consideration of the components of cellular systems, Introduction to co-channel interference, co-channel measurement design of antenna system, antenna parameter and their effects.

[No. of Hrs.: 10]

UNIT – II

Cell Coverage for Signal & antenna structures

General introduction, obtaining the mobile point to point mode, propagation over water or flat open area, foliage loss, propagation near in distance, long distance propagation, point to point prediction model – characteristics, cell site, antenna heights and signal coverage cells, mobile to mobile propagation, Characteristics of basic antenna structures, antenna at cell site, mobile antennas.

Frequency Management and Channel Assignment, Hand Off and Dropped Calls[

Frequency management, fixed channel assignment, non-fixed channel assignment, traffic & channel assignment, Why hand off, types of handoff and their characteristics, dropped call rates & their evaluation. **[No. of Hrs.: 10]**

UNIT – III

Modulation methods and coding for error detection and correlation

Introduction to Digital modulation techniques, modulation methods in cellular wireless systems, OFDM, Block coding, convolution coding and Turbo coding.

Multiple access techniques: FDMA, TDMA, CDMA

Time – division multiple access (TDMA), code division multiple access (CDMA), CDMA capacity, probability of bit error considerations, CDMA compared with TDMA. **[No. of Hrs.: 10]**

UNIT – IV

Second generation, digital, wireless systems

GSM, IS_136 (D-AMPS), IS-95, Mobile management, voice signal processing and coding.

[No. of Hrs.: 10]

TEXT BOOKS:

1. C. Y. Lee and William, "Mobile Cellular Telecommunications", 2nd Ed, McGraw Hill. 2001
2. Mischa Schwartz, "Mobile Wireless Communications", Cambridge Univ. Press, UK, 2005.

REFERENCES:

1. Mobile Communication Hand Book", 2nd Edition, IEEE Press. 2002
2. Theodore S Rappaport, "Wireless Communication Principles and Practice", 2nd Ed, Pearson Education. 2002
3. Lawrence Harte, "3G Wireless Demystified", McGraw Hill Publications. 2000
4. Kaveh Pahlavan and Prashant Krishnamurthy, "Principles of Wireless Networks", PHI.2000

Paper Code:ITW – 706 **L T C**
Paper: Multimedia Technology **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction:

Concept of Multimedia, Multimedia Applications, Hardware Software requirements, Multimedia products & its evaluation.

Components of multimedia: Text, Graphics, Audio, Video., Compression techniques

[No. of Hrs.: 10]

UNIT – II

Animation:

Introduction, Basic Terminology techniques, Motion Graphics 2D & 3D animation.

Introduction to MAYA (Animating Tool): **[No. of Hrs.: 10]**

UNIT – III

Fundamentals, Modeling: NURBS, Polygon,Subdivisions,Organic, animation, paths & bones, deformers. **[No. of Hrs.: 10]**

UNIT – IV

Working with MEL: Basics & Programming,Dynamics

Rendering & Special Effects: Shading & Texturing Surfaces, Lighting, Special effects.

[No. of Hrs.: 10]

TEXT BOOKS:

1. David Hillman, "Multimedia Technology & Applications", Galgotia Publications,2000
2. Rajneesh Agrawal, "Multimedia Systems", Excel Books,2000

REFERENCES:

1. Nigel Chapman & Jenny Chapman, "Digital Multimedia", Wiley Publications. 2000
2. .P. Mukherjee, "Fundamentals of Computer Graphics and Multimedia", PHI. 2001
3. Alias waveport manuals 2004

Paper Code:ITW- 708 **L T C**
Paper: VLSI Design **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction to Transistor Theory: BJT, FET, MOSFET, Introduction to CMOS circuits: MOS Transistors, MOS transistor switches, CMOS Logic, The inverter, Combinational Logic, NAND gate, NOT Gate, Compound Gates, Multiplexer, Memory-Latches and Registers **[No. of Hrs.: 10]**

UNIT – II

MOS Transistor Theory: nMOS & pMOS Enhancement Transistor, MOS Device Design Equation, CMOS Inverter – DC Characteristics, Static Load MOS Inverter, Differential Inverter, Transmission Gate, Tristate Inverter, Bipolar Devices, BiCMOS Inverter. **[No. of Hrs.: 10]**

UNIT – III

CMOS Processing Technology: Silicon Semiconductor Technology – An Overview, wafer processing, oxidation, epitaxy deposition, Ion-implantation and diffusion, The Silicon Gate Process – Basic CMOS Technology, basic n-well CMOS process, p-well CMOS process, Twin tub process, Silicon on insulator, CMOS process enhancement Interconnect, circuit elements, 3-D CMOS, Layout Design Rule: Layer Representations, CMOS n-well Rules, Design Rule of background scribe line, Layer Assignment, SOI Rule, Latch up, Technology-related CAD Issues. **[No. of Hrs.: 10]**

UNIT – IV

Circuit Characterization and performance estimation: Resistance Estimation, Capacitance Estimation, Inductance, Switching Characteristics, CMOS Gate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, CMOS Circuit and Logic Design: CMOS Logic Gate Design, Basic physical design of simple Gate, CMOS Logic Structure, Clocking Strategies, I/O Structure, Low Power Design. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Neil H E Weste and Kamran Esraghian, "Principles of digital VLSI design – A system perspective", Addison Wesley, 2004

REFERENCES:

1. Demassa & Ciccone, "Digital Integrated Circuits", Willey Pub.
2. Neil H.E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design – A System Perspective", Addison Wesley Pub
3. Wayne Wolf, "Modern VLSI Design: system on silicon", Addison Wesley Longman Publisher
4. Douglas A. Pucknell & Kamran Eshranghian, "Basic VLSI Design", PHI
5. Jan M. Rabaey, "Digital Integrated Circuits: A Design Perspective", PHI
6. Sze, S.M., Wiley, "Semiconductor Devices: Physics And Technology", 1985
7. P Antognetti, G Massobrio, "Semiconductor device modeling with SPICE", McGraw-Hill

Paper Code:ITW - 710 **L T C**
Paper: Real Time Systems and Software **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction, Real-time Versus Conventional Software, Computer Hardware for Monitoring and Control, Software Engineering Issues.

Process and State-based Systems model, Periodic and Sporadic Process, Cyclic Executives, CE definitions and Properties, Foreground-Background Organiazations, Standard OS and Concurrency – Architectures, Systems Objects and Object-Oriented Structures, Abstract Data Types, General Object Classes **[No. of Hrs.: 10]**

UNIT – II

Requirements and Design Specifications: Classification of Notations, Data Flow Diagrams, Tabular Languages, State Machine, Communicating Real Time State Machine- Basic features, Timeing and clocks, Sementics Tools and Extensions, Statecharts-Concepts and Graphical Syntax, Semantics and Tools

Declarative Specifications: Regular Expressions and Extensions, Traditional Logics-Propositional Logic, Predicates, Temporal logic, Real time Logic **[No. of Hrs.: 10]**

UNIT – III

Deterministic Scheduling : Assumptions and Candidate Algorithms, Basic RM and EDF Results, Process Interactions-Prority Inversiotn and Inheritance

Execution Time Prediction: Measurement of Software by software, Program Analysis with Timing Schema, Schema Concepts, Basic Blocks, Statements and Control, Schema Practice, Prediction by optimisation, System Interference and Architectural Complexities

Timer Application, Properities of Real and ideal clocks, Clock Servers – Lamport's Logical clocks, Monotonic Clock service, A software Clock server, Clock Synchronization- Centralized Synchronization, Distributed Synchronization **[No. of Hrs.: 10]**

UNIT – IV

Programming Languages: Real Time Language Features, Ada-Core Language, Annex Mechanism for Real Time Programming, Ada and Software Fault Tolerance, Java and Real-time Externsions, CSP and Occam

Operating Systems: Real Time Functions and Sevices, OS Architectures-Real Time UNIX and POSIX, Issues in Task management- Processes and Threads, Scheduling, Synchronization and communication **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Alan C. Shaw, "Real – Time Systems and software", John Wiley & Sons Inc,2001

Paper Code:ITW – 712 **L T C**
Paper: Data Warehousing and Data Mining **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

The Compelling Need for data warehousing: Escalating Need for strategic information, failures of Past decision-support systems, operational versus decision-support systems, data warehousing – the only viable solution, data warehouse defined

Data warehouse – The building Blocks: Defining Features, data warehouses and data marts, overview of the components, metadata in the data warehouse

Defining the business requirements: Dimensional analysis, information packages – a new concept, requirements gathering methods, requirements definition: scope and content

[No. of Hrs.: 10]

UNIT – II

Principles of dimensional modeling: Objectives, From Requirements to data design, the STAR schema, STAR Schema Keys, Advantages of the STAR Schema

Dimensional Modeling:

Updates to the Dimension tables, miscellaneous dimensions, the snowflake schema, aggregate fact tables, families of STARS **[No. of Hrs.: 10]**

UNIT – III

OLAP in the Data Warehouse:

Demand for Online analytical processing, need for multidimensional analysis, fast access and powerful calculations, limitations of other analysis methods, OLAP is the answer, OLAP definitions and rules, OLAP characteristics, major features and functions, general features, dimensional analysis, what are hypercubes? Drill-down and roll-up, slice-and-dice or rotation, OLAP models, overview of variations, the MOLAP model, the ROLAP model, ROLAP versus MOLAP, OLAP implementation considerations **[No. of Hrs.: 10]**

UNIT – IV

Data Mining Basics: What is Data Mining, Data Mining Defined, The knowledge discovery process, OLAP versus data mining, data mining and the data warehouse, Major Data Mining Techniques, Cluster detection, decision trees, memory-based reasoning, link analysis, neural networks, genetic algorithms, moving into data mining, Data Mining Applications, Benefits of data mining, applications in retail industry, applications in telecommunications industry, applications in banking and finance. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Paul Raj Poonia, "Fundamentals of Data Warehousing", John Wiley & Sons, 2003.
2. Sam Anahony, "Data Warehousing in the real world: A practical guide for building decision support systems", John Wiley, 2004

REFERENCES:

1. W. H. Inmon, "Building the operational data store", 2nd Ed., John Wiley, 1999.
2. Kamber and Han, "Data Mining Concepts and Techniques", Hartcourt India P. Ltd., 2001

Paper Code:ITW – 714 **L T C**
Paper: AI & Expert System **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Scope of AI

Games, theorem proving, natural language processing, vision and speech processing, robotics, expert systems, AI techniques- search knowledge, abstraction.

Problem solving

State space search; Production systems, search space control: depth-first, breadth-first search, heuristic search - Hill climbing, best-first search, branch and bound. Problem Reduction, Constraint Satisfaction End, Means-End Analysis **[No. of Hrs.: 10]**

UNIT – II

Knowledge Representation

Predicate Logic: Unification, modus pones, resolution, dependency directed backtracking.Rule based Systems : Forward reasoning: conflict resolution, backward reasoning: use of no backtrack.

Structured Knowledge Representation: Semantic Nets: slots, exceptions and default frames, conceptual dependency, scripts. **[No. of Hrs.: 10]**

UNIT – III

Handling uncertainty on-Monotonic Reasoning, Probablistic reasoning, use of certainty factors, fuzzy logic. **[No. of Hrs.: 10]**

UNIT – IV

Learning

Concept of learning, learning automation, genetic algorithm, learning by inductions, neural nets.

Expert Systems

Need and justification for expert systems, knowledge acquisition, Case studies: MYCIN, RI.

[No. of Hrs.: 10]

TEXT BOOKS:

1. E. Rich and K. Knight, "Artificial intelligence", TMH, 2nd ed., 1992.
2. N.J. Nilsson, "Principles of AI", Narosa Publ. House, 1990.

REFERENCES:

1. D.W. Patterson, "Introduction to AI and Expert Systems", PHI, 1992.
2. Peter Jackson, "Introduction to Expert Systems", AWP, M.A., 1992.
3. R.J. Schalkoff, "Artificial Intelligence - an Engineering Approach", McGraw Hill Int. Ed., Singapore, 1992.
4. M. Sasikumar, S. Ramani, "Rule Based Expert Systems", Narosa Publishing House, 1994

Paper Code:ITW – 716 **L T C**
Paper: Digital Signal Processing **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Discrete time signals and systems, Z-transforms, structures for digital filters, design procedures for FIR and IIR filters. Frequency transformations: linear phase design; DFT. Methods for computing FFT. Noise analysis of digital filters, power spectrum estimation.

Signals and signal Processing: characterization & classification of signals, typical Signal Processing operations, example of typical Signals, typical Signals Processing applications.

Time Domain Representation of Signals & Systems: Discrete Time Signals, Operations on Sequences, the sampling process, Discrete-Time systems, Time-Domain characterization of LTI Discrete-Time systems, state-space representation of LTI Discrete-Time systems **[No. of Hrs.: 10]**

UNIT – II

Transform-Domain Representation of Signals: the Discrete-Time Fourier Transform, Discrete Fourier Transform, DFT properties, computation of the DFT of real sequences, Linear Convolution using the DFT. Z-transforms, Inverse z-transform, properties of z-transform, transform domain representations of random signals.

Transform-Domain Representation of LTI Systems: the frequency response, the transfer function, types of transfer function, minimum-phase and maximum-Phase transfer functions, complementary transfer functions, Discrete-Time processing of random signals. **[No. of Hrs.: 10]**

UNIT – III

Digital Processing of Continuous-Time Signals : sampling of Continuous Signals, Analog Filter Design.
Digital Filter Structure: Block Diagram representation, Signal Flow Graph Representation, FIR and IIR Filter Structures, State-space structure. **[No. of Hrs.: 10]**

UNIT – IV

Digital Filter Design: Impulse invariance method of IIR filter design, Bilinear Transform method of IIR Filter Design, Design of Digital IIR notch filters and FIR filter Design.
Applications of DSP. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Sanjit K. Mitra, “Applications of DSP a Computer based approach” , TMH. 2003
2. Allan Y. Oppenhein & Ronald W. Schater, "Digital Signal Processing”, PHI, 2002

Paper Code:ITW – 718 **L T C**
Paper: Theory of Computation **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Review of basic concepts: Graphs, Trees, Strings, Mathematical Induction, finite State Machine, types of languages and Grammars.

Regular Language, Regular Expression, Regular Grammar, Right and Left Linear Grammar, Closure property of Regular Languages, Pumping Lemma, Properties of Regular expressions, DFA, NFA and their equivalence, Moore's and Mealy machine and their equivalence. identifying non regular languages, reduction of number of states, equivalence between regular language and regular grammars. **[No. of Hrs: 10]**

UNIT – II

Context free Language and Grammar, derivation tree, left most and right most derivation, Parsing and ambiguity, Chomsky and Greibach Normal Form, Pumping Lemma, Properties of CFL including closure property, PDA, NPDA as recognizer of CFL. **[No. of Hrs: 10]**

UNIT – III

Context sensitive language and grammars, matrix Grammar, Markov algorithm, Recursive and recursively enumerable languages, recursive functions, ackerman's functions. **[No. of Hrs: 10]**

UNIT – IV

Turing machine and thesis, Non Deterministic Turing Machine, Universal Turing Machine, computability and Decidability, Undecidable Problems: Halting Problem of TM, Post-correspondence problem, undecidable problems of CFL, Post Systems. Computational Complexity, complexity classes and introduction to P, NP and NP complete.

[No. of Hrs: 10]

TEXT BOOKS:

1. J. E. Hopcroft, J. D. Ulman, "Introduction of automata Theory, Languages and Computation", Student Edition, Norasa, 1979.
2. Zohar Manna, "Mathematical Theory of Computation", McGraw-Hill, 2000

REFERENCES:

1. P. Linz, "An Introduction to formal Languages and Automata", Norasa, 2000.
2. Mishra, Chandrashekharan, "Theory of Computer Science", PHI
3. John C Martin, "Introduction to Theory of formal Languages and Automata", McGraw Hill, 2004.
4. S. P. Eigere Xavier, "Theory of Automata, Formal Languages and Computation, New Age Publishers, 1st Edition, 2004.

Paper Code:ITW-720 **L T C**
Paper: Internet and Web Technology **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Overview of Internet & Web: Basics Concepts of Internet & Web

Web Design : Key issues in web site design , Introduction to HTML, Structure of a Web Page , Various HTML Tags, Table Handling , Frames, Forms & Interactivity. **[No. of Hrs.: 10]**

UNIT – II

Web design Tools : Usage of various web based tools like Microsoft Front page, Adobe Photoshop, Ulead Gif Animator, Macromedia Flash etc.

Security: Various Security methods like firewalls etc . **[No. of Hrs.: 10]**

UNIT – III

E-Commerce: Types of E-Commerce applications, Architectural Framework & Order Management Cycle of E-Commerce, Components and public issues of i-way , media convergence, challenge response system, Electronic Market place, types of electronic payment systems and electronic tokens, challenges in electronic payment systems, Mercantile process and Mercantile consumer Models.

M-Commerce: WAP features and applications, WAP Architecture & Workability, WML skeleton framework. **[No. of Hrs.: 10]**

UNIT – IV

Web Technologies: Brief Overview & usage of various web technologies.

ASP: ASP Application Development Framework - ASP request object, ASP response object, ASP server object, ASP session object, ASP components, Creating interactive applications using active server pages.

JAVA: Embedding java applets and jeva script in web page.

.NET technology & C# - Overview

Web Engineering & Semantic Web: Upcoming Concepts & Research in Web Engineering & Semantic Web. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Internet and Web Technologies by Raj Kamal , TMH,2002
2. World Wide Web Design by C Xavier, TMH,2001
3. Web publishing by Monica D'Souza , TMH,2001
4. Active Server Pages by Heith Morneau, Vikas Publishing House,2000
5. Frontiers of electronic commerce, Ravi Kalkota, Addison Wesley, 2000

REFERENCES:

1. Web Design by David Crowder and Rhonda Crowder, IDG Books India, 2001
2. Database Driven Web Sites by Mike Morrison , Vikas Publishing House, 2003
3. Mark Swank & Drew Kittel, "World Wide Web Database", Samsnet, 2001.
4. ASP 3 Programming , Eric A. Smith , IDG Books India. 2000

Paper Code:ITW – 722 **L T C**
Paper: Network Security **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Basic concepts:

Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS,, Targets: Hardware, Software, Data communication procedures

Threats to Security:

Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security. **[No. of Hrs.: 10]**

UNIT – II

Encryption Techniques:

Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management. **[No. of Hrs.: 10]**

UNIT – III

Message Authentication and Hash Algorithm:

Authentication requirements and functions secue Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service **[No. of Hrs.: 10]**

UNIT – IV

Firewalls and Cyber laws:

Firewalls, Design Princples, Trusted systems, IT act and cyber laws, Virtual private network

Future Threats to Network:

Recent attacks on networks, Case study **[No. of Hrs.: 10]**

TEXT BOOKS:

1. William Stalling “Cryptography and Network Security” Pearson Education,2001

REFERENCES:

1. Charels P. Pfleeger “Security in Computing” Prentice Hall, 2000
2. Jeff Crume “Inside Internet Security” Addison Wesley, 2001

Paper Code: ITW – 724 **L T C**

Paper: Advanced Computer Architecture ` 3 0 3

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Parallel computer models: The state of computing , Multiprocessors and multicomputers, Multivector and SIMD computers, Architectural development tracks

Program and network properties: Conditions of parallelism, Data and resource dependences,Hardware and software parallelism,Program partitioning and scheduling, Grain size and latency, Program flow mechanisms,Control flow versus data flow,Data flow architecture,Demand driven mechanisms,Comparisons of flow mechanisms **[No. of Hrs.: 10]**

UNIT – II

System Interconnect Architectures: Network properties and routing, Static interconnection networks,Dynamic interconnection Networks,Multiprocessor system interconnects,Hierarchical bus systems, Crossbar switch and multiport memory,Multistage and combining network.

Processors and Memory Hierarchy: Advanced processor technology, Instruction-set Architectures,CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors,VLIW Architectures, Vector and Symbolic processors, Memory Technology: Hierarchical memory technology, Inclusion, Coherence and Locality, Memory capacity planning, Virtual Memory Technology **[No. of Hrs.: 10]**

UNIT – III

Backplane Bus System: Backplane bus specification, Addressing and timing protocols, Arbitration transaction and interrupt, Cache addressing models, Direct mapping and associative caches.

Pipelining: Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch handling techniques, Arithmetic Pipeline Design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipelines **[No. of Hrs.: 10]**

UNIT – IV

Vector Processing Principles: Vector instruction types, Vector-access memory schemes.

Synchronous Parallel Processing : SIMD Architecture and Programming Principles, SIMD Parallel Algorithms, SIMD Computers and Performance Enhancement **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Kai Hwang, “Advanced computer architecture”; TMH. 2000
2. D. A. Patterson and J. L. Hennessey, “Computer organization and design”, Morgan Kaufmann, 2nd Ed. 2002

REFERENCES:

1. J.P.Hayes, “computer Architecture and organization”; MGH. 1998
2. Harvey G.Cragon,”Memory System and Pipelined processors”; Narosa Publication. 1998
3. V.Rajaranam & C.S.R.Murthy, “Parallel computer”; PHI. 2002
4. R.K.Ghose, Rajan Moona & Phalguni Gupta, “Foundation of Parallel Processing”, Narosa Publications, 2003
5. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”, MGH. 2001
6. Stalling W, “Computer Organisation & Architecture”, PHI. 2000

7. D.Sima, T.Fountain, P.Kasuk, “Advanced Computer Architecture-A Design space Approach,”Addison Wesley,1997.
8. M.J Flynn, “Computer Architecture, Pipelined and Parallel Processor Design”; Narosa Publishing. 1998
9. D.A.Patterson, J.L.Hennessy, “Computer Architecture :A quantitative approach”; Morgan Kauffmann feb,2002.
10. Hwan and Briggs, “ Computer Architecture and Parallel Processing”; MGH. 1999

Paper Code:ITW – 726 **L T C**
Paper: Robotic Engineering: **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Overview: Historical perspective, classification, applications, components, industrial and technical development. **[No. of Hrs.: 10]**

UNIT – II

Mechanical systems:dynamics, modeling, end effectors.
Drive methods:principles and characteristics. **[No. of Hrs.: 10]**

UNIT – III

Sensors: sensory requirements, available techniques, evaluation selection. Review of control methods.
Computer hardware for robot systems, logic circuits and computer elements, peripheral system organization. **[No. of Hrs.: 10]**

UNIT – IV

Input and output operations and control.
Robot software requirement, functions performed by programming, present robot languages.
Robot vision: capturing the image, frame grabbers, interfacing and controls.

[No. of Hrs.: 10]

TEXT BOOKS:

1. "Robotic Engineering: An integrated approach" by Richard D. Klafter, Thomas A. Chmielewski and Micheal Negin. Prentice Hall India publisher, 2002

REFERENCES:

1. "Robot technology" by Lames G. Keramas. Thomson Publisher, 2003
2. "Fundamentals of robotics analysis and control" by Tsuneo Yoshikawa. Prentice Hall India publishers, 2002

ITW-752: Cellular & Mobile Communivation Lab.
The practical will be based on Cellular & Mobile Communication.

ITW-754: Software Engineering Lab
The practical will be based on Software Engineering.

ITW-756: Elective-I Lab
The practical will be based on Elective-I. If practicals are not possible in any elective course, students are required to do a term paper in the area of chosen elective subjects.

Sr.	**Electives**
1.	Multimedia Technology
1.	VLSI Design
2.	Real Time Systems & Software
3.	Data Warehousing & Data Mining
4.	Artificial Intelligence & Expert System
5.	Digital Signal Processing
6.	Theory of Computation
7.	Internet & Web Technology
8.	Network Security
9.	Advanced Computer Architecture
10.	Robotic Engineering

ITW – 758* Project Work – I
Objective: Students are required select a topic of their interest and develop a minor project on it.

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format (available on www.ipu.ac.in). The student will have to present the progress of the work through seminars. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

*** Non University Exam Scheme**

Paper Code:ITW – 801 **L T C**
Paper: Software Testing **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction: What is software testing and why it is so hard?, Error, Fault, Failure, Incident, Test Cases, Testing Process, Limitations of Testing, No absolute proof of correctness, Overview of Graph Theory. **[No. of Hrs.: 10]**

UNIT - II

Functional Testing: Boundary Value Analysis, Equivalence Class Testing, Decision Table Based Testing, Cause Effect Graphing Technique.

Structural Testing: Path testing, DD-Paths, Cyclomatic Complexity, Graph Metrics, Data Flow Testing, Mutation testing. **[No. of Hrs.: 10]**

UNIT - III

Reducing the number of test cases:

Prioritization guidelines, Priority category, Scheme, Risk Analysis, Regression Testing, Slice based testing

Testing Activities: Unit Testing, Levels of Testing, Integration Testing, System Testing, Debugging, Domain Testing. **[No. of Hrs.: 10]**

UNIT - IV

Object Oriented Testing: Issues in Object Oriented Testing, Class Testing, GUI Testing, Object Oriented Integration and System Testing.

Testing Tools: Static Testing Tools, Dynamic Testing Tools, Characteristics of Modern Tools.

[No. of Hrs.: 10]

TEXT BOOKS:

1. William Perry, "Effective Methods for Software Testing", John Wiley & Sons, New York, 1995.
2. Louise Tamres, "Software Testing", Pearson Education Asia, 2002
3. Robert V. Binder, "Testing Object-Oriented Systems-Models, Patterns and Tools", Addison Wesley, 1999.

REFERENCES:

1. Cem Kaner, Jack Falk, Nguyen Quoc, "Testing Computer Software", Second Edition, Van Nostrand Reinhold, New York, 1993.
2. K.K. Aggarwal & Yogesh Singh, "Software Engineering", 2nd Ed., New Age International Publishers, New Delhi, 2005
3. Boris Beizer, "Software Testing Techniques", Second Edition, Wiley-Dreamtech India, New Delhi, 2003
4. Boris Beizer, "Black-Box Testing – Techniques for Functional Testing of Software and Systems", John Wiley & Sons Inc., New York, 1995.

Paper Code:ITW – 803 **L T C**
Paper: Neural Networks **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Biological, Analogy, Architecture classification, Neural Models, Learning Paradigm and Rule, single unit mapping and the preception. **[No. of Hrs.: 10]**

UNIT – II

Feed forward networks – Review of optimization methods, back propagation, variation on backpropagation, FFANN mapping capability, Mathematical properties of FFANN's Generalization, Bios & variance Dilemma, Radiol Basis Function networks. **[No. of Hrs.: 10]**

UNIT – III

Recurrent Networks – Symmetric hopfield networks and associative memory, Boltzmann machine, Adaptive Resonance Networks **[No. of Hrs.: 10]**

UNIT – IV

PCA, SOM, LVQ, Hopfield Networks, Associative Memories, RBF Networks, Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Haykin S., "Neural Networks-A Comprehensive Foundations", PHI, New Jersey, 1999.
2. Anderson J.A., "An Introduction to Neural Networks", PHI, 1999.
3. Hertz J, Krogh A, R.G. Palmer, "Introduction to the Theory of Neural Computation",Addison-Wesley, California, 1991.

REFERENCES:

1. Hertz J, Krogh A, R.G. Palmer, "Introduction to the Theory of Neural Computation", Addison-Wesley, California, 1991.
2. Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications and Programming Techniques", Addison-Wesley, Reading, Mass, 1992.
3. Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge, MA, 1996.
4. Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York, 1998.
5. Anderson J.A., E. Rosenfield, "Neurocomputing: Foundatiions of Research, MIT Press, Cambridge, MA, 1988.
6. Kohonen T., "Self-Organizing Maps", 2nd Ed., Springer Verlag, Berlin, 1997.
7. Patterson D.W., "Artificial Neural Networks: Theory and Applications", PHI, Singapore, 1995.
8. Vapnik V.N., "Estimation of Dependencies Based on Empirical Data", Springer Verlag, Berlin, 1982.
9. Vapnik V.N., "The Nature of Statistical Learning Theory", Springer Verlag, New York, 1995.
10. Vapnik V.N., "Statistical Learning Theory: Inference from Small Samples", John Wiley, 1998.

Paper Code:ITW - 805 **L T C**
Paper: Embedded System Design **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction to an embedded systems design: Introduction to Embedded system, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES. **[No. of Hrs.: 10]**

UNIT – II

Processes and Operating Systems: Inter-process Communication and Synchronization of Processes, Tasks and Threads, Problem of Sharing Data by Multiple Tasks, Real Time Operating Systems, Basic Concept, OS Services, I/O Subsystems, Interrupt Routines in RTOS Environment, RTOS Task Scheduling model, Interrupt Latency and Response times of the tasks. **[No. of Hrs.: 10]**

UNIT – III

Microcontroller: Microcontroller and Embedded Processors,Overview of 8051 Microcontroller family: Architecture, basic assembly language programming concepts, Instruction set, Addressing Modes, Logical Operation, Arithmetic instructions and programs, Subroutine, Single-bit Instructions and Programming Interrupt Programming, Timer/Counter programming in the 8051, 8051 Serial data with CDS, ADC and Sensors, Stepper Motor, External Memories. Communication programming **[No. of Hrs.: 10]**

UNIT – IV

Networks for Embedded Systems: The I^2C Bus, The CAN bus, SHARC link Ports, Ethernet, Myrinet, Internet

Introduction to Bluetooth: Specification, Core Protocol, Cable replacement protocol. IEEE 1149.1 Testability: Boundary Scan Architecture (JTAG) **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Embedded Systems by Raj Kamal, TMH,2004
2. The 8051 Microcontroller and Embedded Systems by M.A. Mazidi and J. G. Mazidi, Pearson Education press,PHI,2004

REFERENCES:

1. An Embedded Software Primer by David E. Simon, Pearson Education, 2001
2. The 8051 Microcontroller by K.J. Ayala, Penram International, 2000
3. 8051 Microcontroller & Embedded Systems by Dr. Rajiv Kapadia, Jaico Press, 2003
4. Designing Embedded Hardware by John Catsoulis, O'reilly, 2002
5. Embedded System Design by Frank Vahid, Tony Givargis,", John Wiley & Sons, Inc, 2001
6. Building Embedded Linux Systems by Karim Yaghmour, O'reilly, 2001
7. Programming Embedded Systems by Michael Barr, O'reilly, 2002
8. Embedded Ethernet and Internet Complete by Jan Axelson, Penram Publisher. 2000
9. Computers as Components by Wayne Wolf, Harcourt India Pvt. Ltd., 2002

Paper Code:ITW – 807 **L T C**
Paper: Fuzzy Logic **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Classical and Fuzzy Sets:Overview of Classical Sets, Membership Function, α-cuts, Properties of α-cuts, Decomposition Theorems, Extension Principle.

Operations on Fuzzy Sets:
Compliment, Intersections, Unions, Combinations of Operations, Aggregation Operations.

[No. of Hrs.: 10]

UNIT – II

Fuzzy Arithmetic:
Fuzzy Numbers, Linguistic Variables, Arithmetic Operations on intervals & Numbers, Lattice of Fuzzy Numbers, Fuzzy Equations.

Fuzzy Relations:
Crisp & Fuzzy Relations, Projections & Cylindric Extensions, Binary Fuzzy Relations, Binary Relations on single set, Equivalence, Compatibility & Ordering Relations, Morphisms, Fuzzy Relation Equations. **[No. of Hrs.: 10]**

UNIT – III

Possibility Theory:
Fuzzy Measures, Evidence & Possibility Theory, Possibility versus Probability Theory.

Fuzzy Logic:
Classical Logic, Multivalued Logics, Fuzzy Propositions, Fuzzy Qualifiers, Linguistic Hedges.

[No. of Hrs.: 10]

UNIT – IV

Unertainty based Information:
Information & Uncertainity, Nonspecificity of Fuzzy & Crisp sets, Fuzziness of Fuzzy Sets.
Applications of Fuzzy Logic **[No. of Hrs.: 10]**

TEXT BOOKS:

1. G.J.Klir & B.Yuan, "Fuzzy sets & Fuzzy logic," PHI, 1995.

REFERENCES:

1. G.J.Klir & T.A. Folyger,"Fuzzy Sets, Uncertainty & Information", PHI, 1988.
2. Kosko "Neural Networks and Fuzzy System: A Dynamical System Approach to Machine Intelligence"
3. Timothy Ross " Fuzzy Logic and Engineering Application" Tata McGraw Hill

Paper Code:ITW – 809 **L T C**
Paper: Digital Image Processing **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction And Digital Image Fundamentals

The origins of Digital Image Processing, Examples of Fields that Use Digital Image Processing, Fundamentals Steps in Image Processing, Elements of Digital Image Processing Systems, Image Sampling and Quantization, Some basic relationships like Neighbours, Connectivity, Distance Measures between pixels, Linear and Non Linear Operations.

Image Enhancement in the Spatial Domain

Some basic Gray Level Transformations, Histogram Processing, Enhancement Using Arithmetic and Logic operations, Basics of Spatial Filters, Smoothening and Sharpening Spatial Filters, Combining Spatial Enhancement Methods. **[No. of Hrs.: 10]**

UNIT – II

Image Enhancement in the Frequency Domain

Introduction to Fourier Transform and the frequency Domain, Smoothing and Sharpening Frequency Domain Filters, Homomorphic Filtering.

Image Restoration: A model of The Image Degradation / Restoration Process, Noise Models, Restoration in the presence of Noise Only Spatial Filtering, Pereodic Noise Reduction by Frequency Domain Filtering, Linear Position-Invarient Dedradations, Estimation of Degradation Function, Inverse filtering, Wiener filtering, Constrained Least Square Filtering, Geometric Mean Filter, Geometric Transformations. **[No. of Hrs.: 10]**

UNIT – III

Image Compression

Coding, Interpixel and Psychovisual Redundancy, Image Compression models, Elements of Information Theory, Error free comparison, Lossy compression, Image compression standards.

Image Segmentation: Detection of Discontinuities, Edge linking and boundary detection, Thresholding, Region Oriented Segmentation, Motion based segmentation. **[No. of Hrs.: 10]**

UNIT – IV

Representation and Description

Representation, Boundary Descriptors, Regional Descriptors, Use of Principal Components for Description, Introduction to Morphology, Some basic Morphological Algorithms.

Object Recoginition: Patterns and Pattern Classes, Decision-Theoretic Methods, Structural Methods. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Rafael C. Conzalez & Richard E. Woods, "Digital Image Processing", 2nd Ed, Pearson Education. 2004
2. A.K. Jain, "Fundamental of Digital Image Processing", PHI. 2003

REFERENCES:

1. Rosefield Kak, "Digital Picture Processing", 1999
2. W.K. Pratt, "Digital Image Processing", 2000

Paper Code:ITW – 811 **L T C**
Paper: Designing with ASICs **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Types of ASICs – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers. **[No. of Hrs.: 10]**

UNIT – II

ASIC Library design: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC. **[No. of Hrs.: 10]**

UNIT – III

Low level design entry: Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and verilog. **[No. of Hrs.: 10]**

UNIT – IV

Logic synthesis in verilog and & VHDL simulation.

ASIC Construction – Floor planning & placement – Routing. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. J.S. Smith, "Application specific Integrated Circuits", Addison Wesley, 1997.

Paper Code:ITW – 813 **L T C**
Paper: Object Oriented Software Engineering **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction to Software Engineering: Software Engineering Development, Software Life Cycle Models, Comparison of various models

Requirement Elicitation: Introduction to Object Oriented Methodology, Overview of Requirements Elicitation, Requirements Model-Action & Use cases, Requirements Elicitation Activities, Managing Requirements Elicitation. **[No. of Hrs.: 10]**

UNIT – II

Architecture: Introduction, System development is model building, model architecture, requirements model, analysis model, the design model, the implementation model, test model

Analysis: Introduction, the requirements model, the analysis model

[No. of Hrs.: 10]

UNIT – III

Construction: Introduction, the design model, block design, working with construction

Testing: introduction, on testing, unit testing, integration testing, system testing, the testing process **[No. of Hrs.: 10]**

UNIT – IV

Modelling with UML: Basic Building Blocks of UML, A Conceptual Model of UML, Basic Structural Modeling, UML Diagrams.

Case Studies **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Ivar Jacobson, "Object Oriented Software Engineering", Pearson, 2004.
2. Grady Booch, James Runbaugh, Ivar Jacobson, "The UML User Guide", Pearson, 2004.

REFERENCES:

1. Stephen R. Scach, "Classical & Object Oriented Software Engineering with UML and Java: McGraw Hill, 1999.
2. Richard C. Lee, William M. Tepfenhard, "UML and C++, A Practical guide to object-oriented Development", Pearson

Paper Code:ITW – 815 **L T C**
Paper: Cognitive Psychology **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

A Brief history of the cognitive approach, cognitive science, Neuro science, Artificial intelligence, The Parallel processing approach.

Perceptual Process: Perception, pattern recognition, theories of pattern recognition, Bottom-up vs Top-down Processing, Template matching, feature analysis, prototype matching, pattern recognition: The role of the perceives. **[No. of Hrs.: 10]**

UNIT – II

Communication and Language Processing: Linguistic Hierarchy, Chomsky's theory of grammer, Psycho-linguistic aspects, Abstraction of linguistic ideas, knowledge and comprehension, non-verbal abstraction – musical syntax, The language of motion. **[No. of Hrs.: 10]**

UNIT – III

Memory Modules: Memory, process, storage, Short term memory, long term memory, organization in memory, simulation modules of learning and memory, mnemonics, syntactic and semantic issues, Concept formation, problem solving. **[No. of Hrs.: 10]**

UNIT – IV

Contribution of cognitive psychology to advances in Artificial Intelligence, computer based learning/teaching systems, knowledge acquisition and knowledge based systems, expert systems. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Marc de May, "The cognitive Paradigm", Reidel, 1982
2. R. C. Shank, P. Childers, "Cognitive computer on language, Learning and AI", 1984
3. P.C. Kendall, "Advances in Cognition behavioural research and therapy", Academic Press, 1984.

REFERENCES:

1. Solso, R.L. "Cognitive Psychology (3rd Edition), 1991, Allyn & Balon. 1999
2. Matlin M.W., "Cognition (3rd Edition), 1995, Harcourt Brace (Prism Indian Edition). 2000
3. Leahey T.H. & Harris R.J., "Learning and Cognition (4th Edition), PHI,1997

Paper Code:ITW – 817 **L T C**
Paper: Requirement and Estimation Techniques **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Requirements engineering: Requirements Elicitation, Requirement Elicitation techniques, Requirement Analysis, Requirement Analysis Models, Requirement Documentation, Requirement Management, IEEE Std. For SRS **[No. of Hrs.: 10]**

UNIT - II

Size Estimation: Function Point Analysis, Mask II FPA, LOC estimation, Conversion between size measures **[No. of Hrs.: 10]**

UNIT - III

Effort, schedule & cost estimation: Estimation factors, COCOMO-II, Putnam Estimation Model, Estimation by Analogy, Validating Software Estimates **[No. of Hrs.: 10]**

UNIT - IV

Introduction to software life cycle, management activities in software project
Tools: Software Estimation Tools

Industry Resources; IFPUG, UQAM-SEMRL, COSMIC, IEEE, COCOMO **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Swapna Kishore, Rajesh Naik, “Software Requirements and Estimation”, TMH, 1992.

REFERENCES:

1. K.K. Aggarwal & Yogesh Singh, "Software Engineering", 2nd Ed., New Age International Publishers, New Delhi, 2005.
2. Roger Pressman, “Software Engineering: A Practitioiner’s Approach”, 3rd Edition, McGraw Hill, 1992.

Paper Code:ITW – 819 **L T C**
Paper: Digital VLSI Design **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction to Transistor Theory:BJT,FET,MOSFET, Introduction to CMOS circuits: MOS Transistors, MOS transistor switches, CMOS Logic, The inverter, Combinational Logic, NAND gate, NOT Gage, Compound Gates, Multiplexer, Memory-Latches and Registers. **[No. of Hrs.: 10]**

UNIT – II

MOS Transistor Theory. NMOS & pMOS Enhancement Transistor, MOS Device Design Equation, CMOS Inverter – DC Characteristics, Static Load MOS Inverter, Differential Inverter, Transmission Gate, Tristate Inverter, Bipolar Devices, BiCMOS Inverter. **[No. of Hrs.: 10]**

UNIT – III

CMOS Porcessing Technology: Silicon Semiconductor Technology – An Overview, wafer processing, oxidation, epitaxy deposition, Ion-implantation and diffusion. The Silicon Gate Process-Basic CMOS Technology, basic n-well CMOS process, p-well CMOS process, Twin tub process, Silicon on insulator, CMOS process enhancement-Interconnect, ciecuit elements, 3-D CMOS, Layout Design Rule: Layter Represenттions, CMOS n-well Rules, Design Rule of background scribe line, Layer Assignment, SOI Rule, Latch up, Technology-related CAD Issues **[No. of Hrs.: 10]**

UNIT – IV

Circuit Characterization and performance estimation:Resistance Estimation, Capacitance Estimation, Inductance, Switching Characteristics, CMOS Gate Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing, CMOS Circuit and Logic Design: CMOS Logic Gate Design, Basic physical design of simple Gate, CMOS Logic Structure, Clocking Strategies, I/O Structure, Low Power Design. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Principles of CMOS VLSI Design – A System Perspective by Neil H.E.Weste and Kamran Eshraghian;Addison Wesley Pub.,2004

REFERENCES:

1. Digital Integrated Circuits by Demassa & Ciccone, Willey Pub. 2002
2. Modern VLSI Design: system on silicon by Wayne Wolf;Addison Wesley Longman Publisher, 2001
3. Digital Integrated Circuits by J.M. Rabaey; PHI, 2003
4. Introduction to VLSI Circuits and Systems by J.P. Uyemura, Wiley Pub. 2002
5. Basic VLSI Design by Pucknell & Eshraghian;PHI, 2001`
6. microelectronics by Jacob Millman and Arvin Grabel, TMH, 2000
7. Semi conductor devices and technology by S.M. Sze, TMH, 2001
8. VLSI technology, by S.M. Sze, TMH, 2000

Paper Code:ITW – 821 **L T C**
Paper: Telecommunication Networks **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Evolution of Tele-Communication Networks, Basic Switching System, Simple Tele-phone Communication, Brief Introduction to Electromagnetic Exchanges, Electronic Switching – Space Division Switching Stored Programme Control – Centralized SPC, Distributed SPC, Software Architecture, Application Software – Enhanced Services, Multi Stage Switching Networks.

[No. of Hrs.: 10]

UNIT – II

Speech Digitization, Quantization Noise, Componding, Differential Coding, Delta Modulation, Vocodors, Pulse Transmission on Transmission line concepts, Line Coding, NRZ and RZ Codes, Manchester Coding, AMI Coding, Walsh Codes, TDM, **[No. of Hrs.: 10]**

UNIT – III

Time Division Switching – Time Division space switching, Time Division Time Switching, Time multiplexed space switching, Time multiplexed Time Switching, Combination Switching.

Traffic Engineering, Grade of Service and Blocking Probabity – Telephone Networks, Subscriber Loops, Switching Hierchy and Routing, Transmission Plans and Systems, Signaling Techniques, In Channel, Common Channel. **[No. of Hrs.: 10]**

UNIT – IV

Access Technology; WLL, (Wire less loop), ADSL (Asymmetrical Digital Subscriber Loop) AVCC(Advanced Intelligent Network), BMFB

Wired, Wireless, broadcast, point to point, Satellite medium-SCPC, VSAT broadcast medium etc, link budget analysis, Link behavior, Peburst, error, Optimum packet size, error control, Elementary coding ideas , ATM transport mechanism, ISDN **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Networkd, T. Viswanathan, “Telecommunication Switching Systems”, PHI, 2003.
2. J.E.Flood, “Telecoomunications Switching Traffic and Networks” 1999

Paper Code:ITW – 823 **L T C**
Paper: Programming with AVR microcontroller **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Microcontroller architecture, The AVR RISC Microcontroller Architecture: AVR family architecture, Register File, Memory access and instruction Execution, I/O Memory, I/O Ports.

[No. of Hrs.: 10]

UNIT – II

AVR Instruction Set: Program and data addressing modes, Arithmetic & Logic Instruction, Program Control Instruction, Data Transfer Instruction

AVR Hardware Design Issues: Power source, Operating clock sources, Reset circuit

[No. of Hrs.: 10]

UNIT – III

Hardware & Software Interfacing with AVR: Lights & switches, Stack operation in AVR Processors, Implementing Combinational Logic, Connecting the AVR to the PC serial port, Expanding I/O, Interfacing analog to Digital converters and DAC, Interfacing with LED/LCD displays, Stepper motor interface with AVR. **[No. of Hrs.: 10]**

UNIT – IV

Communication links for the AVR Processor: RS-232 Link, RS-422/423 link, SPI and microwave bus, IrDA Data link, CAN

AVR System Development tool: Code assembler, Code simulator, Evaluation boards, AVR emulator, Device Programmer **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Dhananjay V. Gadre, "Programming and Customizing the AVR Microcontroller", TMH 2003

Paper Code:ITW – 825 **L T C**
Paper: Natural Language Processing & Understanding **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introcution to NLP and NLU – Applications of NLP & NLU, open problem, Differences levels of Language Analysis **[No. of Hrs.: 10]**

UNIT – II

Syntatic processing – Linguistic Background – Outline of English Syntax, Top down & Bottom up processing, Finite state models and morphological processing.
Grammer for Natural language, Ambiguity Resolution. **[No. of Hrs.: 10]**

UNIT – III

Semantic Introduction – Semantic and logical form, Ambiguity, speech acts and embedded Sentences, other strategies for Sementic Interpretation. **[No. of Hrs.: 10]**

UNIT – IV

Speech Recognition and Spoken language – Issue in Speech Recognition sound structure, Signal processing, HMM model, NLP, NLU and speech Recognition. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. James Allen, "Natural Language Understanding", Pearson education, 2003
2. Rajeev S., Zevarsky, "Speech processing and Recognition , PHI, 2000

Paper Code: ITW – 827 **L T C**
Paper: Enterprise Resource Planning **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction:

ERP: An Overview, Enterprise-An Overview, Benefits of ERP, ERP and Related Technologies, Business Process Reengineering (BPR), Data Warehousing, Data Mining, On-line Analytical Processing (OLAP), Supply Chain Management **[No. of Hrs.: 10]**

UNIT – II

ERP Implementation:

To be or not to be, ERP Implementation Lifecycle, Implementation Methodology, Not all Packages are Created Equal!, ERP Implementation-The Hidden Costs, Organizing the Implementation, Vendors, Consultants and Users, Contracts with Vendors, Consultants and Employees, Project Management and Monitoring, After ERP Implementation. **[No. of Hrs.: 10]**

UNIT – III

The Business Modules:

Business Modules in an ERP Package, Finance, Manufacturing (Production), Human Resources, Plant Maintenance, Materials Management, Quality Management, Sales and Distribution

[No. of Hrs.: 10]

UNIT - IV

The ERP Market:

ERP Market Place, SAP AG, PeopleSoft, Baan Company, JD Edwards World Solutions Company, Oracle Corporation, QAD, System Software Associates, Inc. (SSA)

ERP-Present and Future:

Turbo Charge the ERP System, Enterprise Integration Applications (EIA), ERP and E-Commerce, ERP and Internet, Future Directions in ERP, Appendices" **[No. of Hrs.: 10]**

TEXT BOOKS:

1. S. Sadagopan, “Enterprise Resource Planning”, Tata McGraw Hill 2000
2. Alexis Leon, “Enterprise Resource Planning”, Tata McGraw Hill 2001

Paper Code:ITW – 829 **L T C**
Paper: Soft Computing **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Neural Networks: History, overview of biological Neuro-system, Mathematical Models of Neurons, ANN architecture, Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning, ANN training Algorithms-perceptions, Training rules, Delta, Back Propagation Algorithm, Multilayer Perceptron Model, Hopfield Networks, Associative Memories, Applications of Artificial Neural Networks. **[No. of Hrs.: 10]**

UNIT – II

Fuzzy Logic: Introduction to Fuzzy Logic, Classical and Fuzzy Sets: Overview of Classical Sets, Membership Function, Fuzzy rule generation.

Operations on Fuzzy Sets: Compliment, Intersections, Unions, Combinations of Operations, Aggregation Operations. **[No. of Hrs.: 10]**

UNIT – III

Fuzzy Arithmetic: Fuzzy Numbers, Linguistic Variables, Arithmetic Operations on Intervals & Numbers, Lattice of Fuzzy Numbers, Fuzzy Equations.

Fuzzy Logic: Classical Logic, Multivalued Logics, Fuzzy Propositions, Fuzzy Qualifiers, Linguistic Hedges.

Uncertainty based Information: Information & Uncertainty, Nonspecificity of Fuzzy & Crisp Sets, Fuzziness of Fuzzy Sets. **[No. of Hrs.: 10]**

UNIT – IV

Introduction of Neuro-Fuzzy Systems, Architecture of Neuro Fuzzy Networks.

Application of Fuzzy Logic: Medicine, Economics etc.

Genetic Algorithm: An Overview, GA in problem solving, Implementation of GA

[No. of Hrs.: 10]

TEXT BOOKS:

1. Anderson J.A, "An Introduction to Neural Networks",PHI, 1999.
2. Hertz J. Krogh, R.G. Palmer, "Introduction to the Theory of Neural Computation", Addison-Wesley, California, 1991.
3. G.J. Klir & B. Yuan, "Fuzzy Sets & Fuzzy Logic", PHI, 1995.
4. Melanie Mitchell, "An Introduction to Genetic Algorithm", PHI, 1998.

REFERENCES:

1. "Neural Networks-A Comprehensive Foundations", Prentice-Hall International, New Jersey, 1999.
2. Freeman J.A. & D.M. Skapura. "Neural Networks: Algorithms, Applications and Programming Techniques", Addison Wesley, Reading, Mass, (1992).

Paper Code:ITW – 831 **L T C**
Paper: Software Quality Assurance & Certification **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Concepts and Overview: Concepts of Software Quality, Quality Attributes, Software Quality Control and Software Quality Assurance, Evolution of SQA, Major SQA activities, Major SQA issues, Zero defect Software.

Software Quality Assurance: The Philosophy of Assurance, The Meaning of Quality, The Relationship of Assurance to the Software Life - Cycle, SQA Techniques. **[No. of Hrs.: 10]**

UNIT – II

Tailoring the Software Quality Assurance Program: Reviews, Walkthrough, Inspection, and Configuration Audits.

Evaluation: Software Requirements, Preliminary design, Detailed design, Coding and Unit Test, Integration and Testing, System Testing, types of Evaluations. **[No. of Hrs.: 10]**

UNIT – III

Error Reporting: Identification of Defect, Analysis of Defect, Correction of Defect, Implementation of Correction, Regression Testing, Categorization of Defect, Relationship of Development Phases.

Trend Analysis: Error Quality, Error Frequency, Program Unit Complexity, Compilation Frequency.

Corrective Action as to Cause: Identifying the Requirement for Corrective Action, Determining the Action to be Taken, Implementing the Correcting the corrective Action, Periodic Review of Actions Taken. **[No. of Hrs.: 10]**

UNIT – IV

Configuration Management: Maintaining Product Integrity, Change Management, Version Control, Metrics, Configuration Management Planning.

Traceability, Records, Software Quality Program Planning, Social Factors: Accuracy, Authority, Benefit, Communication, Consistency, and Retaliation. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. Robert Dunn, "Software Quality Concepts and Plans", Prentice-Hall, 1990.
2. Alan Gillies, "Software Quality, Theory and Management", Chapman and Hall, 1992.

REFERENCES:

1. Michael Dyer, "The Cleanroom approach to Quality Software Engineering", Wiley & Sons, 1992.
2 Daniel Freedman, Gerald Weinberg, "Handbook of Walkthroughts, Inspections and Technical Reviews", Dorset House Publishing, 1990
3. Tom Gilb, "Principles of Software Engineering Management", Addison-Wesley, 1988.
4. Tom Gilb, Dorothy Graham, "Software Inspection" Addison-Wesley, 1993.
5. Watts Humphrey, "Managing the Software Process", Addison-Wesley, 1990.
6. Watts Humphrey, "A Discipline for Software Engineering", Addison-Wesley, 1995.

Paper Code:ITW – 833 **L T C**
Paper: Network Programming **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction

TCP/IP Architecture, TCP/IP addressing, services, FTP, SMTP, TFTP, SNMP, Network file system, domain name system, transport layer protocols, user datagram protocol, transmission control protocol. **[No. of Hrs.: 10]**

UNIT – II

Interprocess communications

File and record locking, pipes, FIFO's, stream and messages, message quues, samphorers.

[No. of Hrs.: 10]

UNIT – III

Sockets

Sockets system cells, reserved parts, stream pipes, socket option, asynchronous I/O, Sockets and signals **[No. of Hrs.: 10]**

UNIT – IV

Transport Lay Interface

Elementary TLI functions, stream and stream pipes, asynchronous I/O I/O multiplexing

Remote Procedure cells **[No. of Hrs.: 10]**

TEXT BOOKS:

1. R. Stevens, "Unix Network Programming", PHI 1998

REFERENCES:

1. A. Stevens, "TCP/IP Illustrated", Vol. 1-3, Addison Wesley, 1998
2. J. Martin, "TCP/IP Networking – Architecture, Administration and programming", Prentice Hall, 1994.
3. D.E. Comer, "Internetworking with TCP/IP, Vol. 1, Principles, Protocols, and architecture, PHI, 2000

Paper Code:ITW - 835 **L T C**
Paper: Advanced VLSI Design **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Integrated Circuit and Modeling: MOS and BJT transistor modelling for MOS transistor & BJT - SPICE modelling parameters – CMOS and bipolar processing – CMOS and Analog layout consideration

Current Mirror: The Cascode connection, sensitivity analysis, Temperature analysis, Transient analysis, Layout of simple current mirror, Matching in MOSFET mirror **[No. of Hrs.: 10]**

UNIT – II

Voltage Dividers: The Resistor-MOSFET Divider, The MOSFET-only Voltage Divider, Current source Self-biasing, Bandgap Voltage References, Beta Multiplier Referenced self-biasing

Amplifiers: Gate-Drain Connected loads-Common Source Amplifiers, The Source follower, Common Gate Amplifier; Current Source Loads-The cascode connection, The Push-pull amplifier; Noise and Distortion in Amplifiers-modeling amplifier noise, class AB amplifier **[No. of Hrs.: 10]**

UNIT – III

Feedback Amplifiers: The feedback equation, properties of negative feedback on amplifier design, Recongnizing feedback topologies, the voltage Amp, The trans-impedance, the Tran conductance, The Current amplifier

Differential Amplifier: The source coupled paier, The Source Cross-coupled pair, Cascode Loads, Wide-swing Differential Amplifier **[No. of Hrs.: 10]**

UNIT – IV

Operational Amplifier: Basic CMOS Op-Amp Design, Operational Trans-conductance Amplifier, The Differential Output Op-Amp **[No. of Hrs.: 10]**

TEXT BOOKS:

1. CMOS Circuit Design, layout and simulation by R.J. Baker, H.W. Li and D.E. Boyce; PHI 2004

REFERENCES:

1. Semiconductor Devices modelling with SPICE by Massobrio and antognehi; McGraw Hill Pub.
2. Operation and modelling o f the MOS transistor by Yannis Tsividis; McGraw Hill Pub.
3. CMOS Analog Circuit Design by Phillips A. Allen and D. R. Holberg; Oxford Univ.
4. VLSI Design Techniques for Analog and Digital Circuits by R.L. Geiger, P.E. Allen and N.R. Strader, MGH

Paper Code:ITW – 837 **L T C**
Paper: Advanced Digital Circuit Design **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Digital design fundamentals: Concept of a logic state – state machine – finite state machine – models for sequential machines – Moore and Mealy machines and memory cells. **[No. of Hrs.: 10]**

UNIT – II

Design of simple FSMS: Glitches – glitch analysis – filtering out Glitches – Guidelines for state code assignment – state diagram from specifications – state assignments – next state and output k maps – asynchronous inputs – debouncing circuit and logic diagram. **[No. of Hrs.: 10]**

UNIT – III

Alternative design methodologies: Conventional approach – using state decoder – direct and indirect addressed multiplexers – direct and indirect addressed FPLA/FROM – Design using shift registers and counters for memory and programmable FSM architecture. **[No. of Hrs.: 10]**

UNIT – IV

Advanced digital concepts: Microinstructions – fixed instruction set – sequencer based design – sequencer with subroutine capability – control sequencer – system level design and functional partition.

Asynchronous sequential circuits: Lumped path delay (LPD) model – problems associated with asynchronous sequential circuits – design of asynchronous circuits – implementation using PLA.

[No. of Hrs.: 10]

TEXT BOOKS:

1. W.I.Fletcher: "An engineering approach to digital design", PHI-1994.

REFERENCES:

1. R.F.Tinder, "Digital engineering design: A modern approach", PHI-1991.

Paper Code:ITW – 839 **L T C**
Paper: Mobile Computing **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Introduction to Personal Communications Services (PCS): PCS Architecture, Mobility management, Networks signalling.

Global System for Mobile Communication (GSM) system overview: GSM Architecture, Mobility management, Network signalling, Performance Analysis: Admission control and handoffs

[No. of Hrs.: 10]

UNIT – II

2.5/3G Mobile Wireless systems: packet switched Data
Introduction, 3G CDMA cellular standards, Wideband Code Division Multiple Access (W-CDMA), and CDMA 2000, Quality of services in 3G. 2.5/3G TDMA: General Packet Radio Services (GRPS) and EDGE. **[No. of Hrs.: 10]**

UNIT – III

Access Scheduling techniques in cellular systems
Slotted Aloha access, integrated access: voice and data, scheduling in packet based cellular systems.
Mobile Data Communication: WLANs (Wireless LANs) IEEE 802.11 standard, Mobile IP.

[No. of Hrs.: 10]

UNIT – IV

Wireless Application Protocol (WAP): The Mobile Internet standard, WAP Gateway and Protocols, wireless mark up Languages (WML).

Wireless Local Loop(WLL): Introduction to WLL Architecture, wireless Local Loop Technologies.

Global Mobile Satellite Systems; case studies of the IRIDIUM and GLOBALSTAR systems.

[No. of Hrs.: 10]

TEXT BOOKS:

1. Yi-Bing and Imrich Chlamtac, "Wireless and Mobile Networks Architectures", John Wiley & Sons, 2001.
2. Raj Pandya, "Mobile and Personal Communication Systems and Services", PHI, 2001
3. Mischa Schwartz, "Mobile Wireless Communications", Cambridge University Press, UK, 2005.

REFERENCES:

1. Mark Ciampa, "Guide to Designing and Implementing wireless LANs", Thomson learning, Vikas Publishing House, 2001.
2. Ray Rischpater, "Wireless Web Development", Springer Publishing, 2000.
3. Sandeep Singhal, "The Wireless Application Protocol", Pearson Education Asia, 2000.
4. P. Stavronlakis, "Third Generation Mobile Telecommunication systems", Springer Publishers, 2001

Paper Code:ITW – 841 **L T C**
Paper:Total Quality Management **3 0 3**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

TQM: An introduction, Leadership for TQM, Laying the foundation of TQM. **[No. of Hrs.: 10]**

UNIT – II

Focus and approach: TQM and improvement Processes, Policy Promotions, Tools and techniques for improvement, Application thrusts and features, Education and training. **[No. of Hrs.: 10]**

UNIT – III

TQM policy and deployment guidelines, Information analysis and information technology..

[No. of Hrs.: 10]

UNIT – IV

Strategic quality planning, management of process quality, organizing for TQM, Cost of quality, effective training for TQM, ISO-9000, Case studies. **[No. of Hrs.: 10]**

TEXT BOOKS:

1. "Total Quality Management" by S.M. Sundara Raju. TMH Publishing Company Ltd. 2000

REFERENCES:

1. Joel E. Ross, "Total Quality Management", Vanity Books International, N. Delhi, 2000
2. G.S. Basodia, "Total Quality Management", Mangaldeep Publisher, Jaipur, 2002

ITW-851: Software Testing Lab.

The practical will be based on Software Testing.

ITW- 853: Elective-II Lab.
The practical will be based on Elective II.

ITW- 855: Elective-III Lab.
The practical will be based on Elective III.

ITW – 857* Project Work – II
Objective: Students are required select a topic of their interest and develop a minor project on it.

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format (available on www.ipu.ac.in). The student will have to present the progress of the work through seminars. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

*** Non University Exam Scheme**

ITW – 802 Dissertations

Objective: Students are required select a topic of their interest and prepare a dissertation on it.

The student will submit a synopsis at the beginning of the semester for the approval from the school project committee in a specified format. Synopsis must be submitted within a two weeks. The first defense, for the dissertation work, should be held with in a one month. Dissertation Report must be submitted in a specified format (available on www.ipu.ac.in) to the school for evaluation purpose.

ITW – 804* Seminar & Progress Report

The student will have to present the progress of the dissertation work through seminars and progress reports at the interval of four weeks during the semester. Minimum two seminar will be held during the semester to assess the progress of dissertation work.

ITW – 806* Comprehensive Viva

Objective: Students are required give viva-voce exam.

*** Non University Exam Scheme**