SCHEME OF EXAMINATION

&

SYLLABI

for

Master of Technology
(VLSI Design)

Regular

GURU GOBIND SINGH
INDRAPRASTHA
UNIVERSITY

Guru Gobind Singh Indraprastha University
Kashmere Gate, Delhi – 110403 [INDIA]
www.ipu.ac.in

.

Eligibility Condition

B. Tech / B.E in Electronics & Communication / Electronics / Computer Science / Information Technology or equivalent degree with 60% marks.

M Sc. Physics (Electronics) / M Sc. Electronics with 60% marks.

Admission Procedure

Admission will be made on the basis of GATE score in the relevant field.

If seats remain vacant after admitting the students with valid GATE score, then the admission will be made on the basis of merit of the qualifying marks subject to minimum 60% marks in the qualifying degree.

SCHEME OF EXAMINATION

Master of Technology
(VLSI Design)

First Semester

Course Code	Subject Name	L	T/P	Credits
Theory Papers				
ITV-601	Digital System Design with Verilog	4	-	4
ITV-603	VLSI Technology	4	-	4
ITV-605	Basic VLSI Design	4	-	4
*ITR-601	Algorithm Analysis and Design	4	-	4
*ITR-605	Advance Computer Architecture	4	-	4
Practical /Viva-voce				
ITV-651	DSD with Verilog Lab	-	2	2
ITV-653	Digital IC design Lab	-	2	2
ITV-655	AAD Lab	-	2	2
Total		20	8	26

Note:
The subjects marked with (*) have been coded uniformly across M. Tech (IT), M. Tech (CSE) and M. Tech (VLSI Design). Minor modifications have been done in the course contents and syllabi of these subjects.

SCHEME OF EXAMINATION
Master of Technology
(VLSI Design)

Second Semester

Course Code	Subject Name	L	T/P	Credits
Theory Papers				
ITV-602	Analog VLSI Design	4	-	4
ITV-604	Advanced VLSI Design	4	-	4
Electives (Choose any Three)				
ITV-606	Computational Technique	4	-	4
ITV-608	Low Power VLSI Design	4	-	4
ITV-610	VLSI Test & Testability	4	-	4
∗ITR-604	Embedded System Design using 8051	4	-	4
ITV-612	Designing with ASICS	4	-	4
∗ITR-610	Digital Signal Processing	4	-	4
*ITR-612	Real Time System & Software	4	-	4
ITV-614	Microwave & Optoelectronic Devices	4	-	4
*ITR-620	Neural Networks	4	-	4
ITV-616	Project Work	4	-	4
Practical / Viva-voce				
ITV-652	Analog VLSI Design	-	2	3
ITV-654	Electives based Lab	-	2	3
Total		20	8	26

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SCHEME OF EXAMINATION
Master of Technology
(VLSI Design)

Third Semester

Course Code	Subject Name	L	T/P	Credits
Theory Papers				
ITV-701	Algorithms for VLSI Design Automation	4	-	4
Electives (Choose any TWO)				
ITV-703	Process, Devices & Circuit Simulation	4	-	4
ITV-705	Nano Technology	4	-	4
ITV-707	Hardware-Software Co-design	4	-	4
ITV-709	Genetic Algorithms for VLSI Design	4	-	4
ITV-711	CMOS RF Circuit Design	4	-	4
ITV-713	Cryptology and Crypto Chip Design	4	-	4
ITV-715	MEMS and IC Integration	4	-	4
ITV-717	Computer Aided VLSI Design	4	-	4
ITV-719	Designing with AVR Microcontroller	4	-	4
ITV-721	Advanced Computational Methods	4	-	4
ITV-723	Project work	4	-	4
*ITR-727	Digital Image Processing	4	-	4
Practical / Viva-voce				
ITV-751	Lab based on Algorithm for VLSI Design automation	-	2	2
ITV-753	Second Elective	-	2	2
ITV-755	Minor Project	-	-	10
Total		12	6	26

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SCHEME OF EXAMINATION
Master of Technology
(VLSI Design)

Fourth Semester

Code No.	Paper	L/P	Credits
ITV 752	Dissertation	-	22
ITV 754**	Seminar & progress Report	-	4
	Total	-	26

Note:
** **Non University Examination system**

1. The total number of credits of the programme M. Tech. [VLSI Design] = 104

2. Each student shall be required to appear for examinations in all courses. However, for the award of the degree a student shall be required to earn the minimum of 100 credits.

Paper Code: ITV - 601	L	T	C
Paper: Digital System Design with Verilog	4	-	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The objective of the course is to introduce basics of digital system design. This course will introduce a number a number of practical issues in digital system design such as device electrical characteristics, I/O behavior, modeling and device interfacing. It will also introduce hardware description language (Verilog) to describe a digital design and discuss design and implementation of combinational and sequential circuits with programmable logic devices such as Field Programmable Gate Array chips (FPGA).

Unit 1

ASIC Design Flow, Introduction to Verilog, Language Constructs and Conventions in Verilog, Gate Level Modeling, Architecture of FPGA

Unit 2

Modeling at Data Flow Level, Continuous Assignment Structures, Delays and Continuous Assisgnments, Assignment to Vectors, Operators, Verilog for combinational Circuits, Design of Adder, Subtractor, Decoders, Encoders, Multiplexer, code Converter.

Unit 3

Behavioral Modeling: Operator and Assignments, Functional Bifurcation, Initial & Always Construct, Assignments with Delays, wait construct, Multiple always blocks, If and if-else, assign-deassign, repeat Construct, Loop Construct: for,while& forever, Parallel blocks, force-release construct, event
Design of Flip flop, Shift register and Counters using Verlilog

Unit 4

Functions, Tasks,user defined primitives, State Machine: Moore and mealay state model, Verilog code for moore-type FSM, Specification of Mealy FSM using Verilog, Mealy-type and Moore-type FSM for Serial Adder

Text Books:

[T1] Fundamental of digital Logic with Verilog design by S. Brown & Z. Vransesic, TMH.
[T2] Design through Verilog HDL by T.R. Padmanabhan & B. Bala Tripura Sundari, Wiley Pub. 2007

Reference Books:

[R1] Digital Design by Frank Vahid, Wiley, 20063.
[R2] Introduction to Digital Systems by M. Ercegovac, T. Lang and L.J. Moreno, Wiley,2000.

Paper Code: ITV-603	L	T	C
Paper: VLSI Technology		4	- 4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: VLSI technology has become a major driving force in the development of all types of electronic systems. This course will introduce the fundamental concepts and techniques involved in the fabrication of VLSI (Very Large Scale Integration) circuits. These include crystal growth, wafer preparation, epitaxy, diffusion, lithography, oxidation, etching etc.

Unit 1

Crystal growth & wafer preparation. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc. (4 lectures)

Epitaxy [T1]

Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure. (6 lectures)

Unit 2

Oxidation [T1]

Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides. Oxidation technique & systems dry & wet oxidation. Masking properties of SiO_2. (4 lectures)

Diffusion [T1]

Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer. (4 lectures)

Unit 3

Lithography [T1]

Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: roster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X ray sources & masks. Ion lithography. (10 lectures)

Unit 4

Etching [T1]

Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & apostrophic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching. (10 lectures)

Text Books

[T1] S.M. Sze, " Modern Semiconductor Device Physics", John Wiley & Sons, 2000.

Reference Books

[R1]B.G. Streetman, "Solid State Electronics Devices", Prentice Hall, 2002.

[R2]Chen,"VLSI Technology" Wiley, March 2003.

Paper Code: ITV-605	L	T	C	
Paper: Basic VLSI Design		4	-	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: Study of: Derive basic analytical MOS circuit equations. Locate information not presented in class, in the library. Analyze circuits using both analytical and CAD tools. Use a design flow to design a CMOS integrated circuit in a team environment. Interpret a design specification. Design test benches which can prove that a design meet a specification. Identify regions where circuit models are valid.

Unit 1

Introduction [T1]: Basic principle of MOS transistor, Introduction to large signal MOS models (long channel) for digital design. (3 lectures)

MOS Circuit Layout & Simulation [T1]: MOS SPICE model, device characterization, Circuit characterization, interconnects simulation. MOS device layout: Transistor layout, Inverter layout, CMOS digital circuit layout & simulation. (4 lectures)

Unit 2

The MOS Inverter [T1]: Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption. (8 lectures)

Unit 3

Combinational MOS Logic Design [T1]

Static MOS design [T1]: Complementary MOS, Ratioed logic, Pass Transistor logic, complex logic circuits. (4 lectures)

Sequential MOS Logic Design [T1]

Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells design (6 lectures)

Unit 4

Dynamic MOS design [T1]: Dynamic logic families and performances. (4 lectures)

Interconnect & Clock Distribution [T1] [T2]

Interconnect delays, Cross Talks, Clock Distribution. Introduction to low power design, Input and Output Interface circuits. (3 lectures)

BiCMOS Logic Circuits [T1]

Introduction, BJT Structure & operation, Basic BiCMOS Circuit behavior, Switching Delay in BiCMOS Logic circuits, BiCMOS Application. (4 lectures)

Text Books

[T1] Kang & Leblebigi "CMOS Digital IC Circuit Analysis & Design"- McGraw Hill, 2003.

[T2] Rabey, "Digital Integrated Circuits Design", Pearson Education, Second Edition, 2003.

Reference Books

[R1] Weste and Eshraghian, "Principles of CMOS VLSI design" Addison-Wesley, 2002.

Paper Code: ITR-601	L	T	C
Paper: Algorithm Analysis and Design	4	0	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The objective of this course is to provide the techniques and theory for designing and analyzing efficient computer algorithms. The design techniques include divide-and-conquer, transform-and-conquer, dynamic programming, greedy techniques, and so on. Algorithms designed by using the techniques for manipulating lists, trees, and graphs, and for solving other problems are described and analyzed. The mathematical methods for analyzing non-recursive and recursive algorithms are discussed. Also, the problems of NP-completeness are addressed.

Unit 1[T1]

Complexity and running times, asymptotic notations, Solution of Recurrence relations, Divide-and-Conquer: Merge sort, Counting Inversions, Finding the closest pair of points, Dynamic programming: basic dynamic programming technique, Solution of Few Problems like Matrix chain multiplication, Longest Common subsequence, dynamic programming on trees, tree decomposition, and algorithms for graphs with bounded tree width. (10 lectures)

Unit 2[T1]

Greedy algorithms: Minimum spanning trees, Huffman codes, matroids, and multicastcost-sharing. Network flows: maximum flows and minimum cuts, the preflow-push algorithm, minimum-cost flows, multicommodity flows, and applications to matching, scheduling, network routing and vision. (10 lectures)

Unit 3[T1]

Time and space measures, hierarchy theorems, complexity classes P, NP, L, NL, PSPACE, BPP and IP, complete problems, P versus NP conjecture, quantiers and games, provably hard problems, relativized computation and oracles, probabilistic computation, interactive proof systems. Approximation algorithms: greedy algorithms, local search, on-line algorithms, primal dual algorithms, linear programming. (10 lectures)

Unit 4[T1]

Randomized algorithms: basic techniques from discrete probability, and applications to optimization, distributed computation, and packet routing. Algorithms in algebra and number theory: Integer arithmetic, Csanky's algorithm, Chistov's algorithm, matrix rank, linear equations and polynomial gcds, FFT, Luby's algorithm, primarily testing. (10 lectures)

Text Books:

[T1] T. H. Cormen, C. E. Leiserson, R.L. Rivest, C. Stein, "Introduction to Algorithms", 2nd Edition, PHI. 2002'

Reference Books:

[R1] A.V. Aho, J. E. Hopcroft, J.D. Ulman, "The Design & Analysis of Computer Algorithms", Addison Wesley. 2000.
[R2] V. Manber, "Introduction to Algorithms – A Creative Approach", Addison Wesley. 1999.
[R3] Ellis Harwitz and Sartaz Sahani, "Fundamentals of Computer Algorithms", Galgotia. 2001.
[R4] John C.Martin, "Introduction to Languages and Theory of Computation", TMH.

Paper Code: ITR-605		L	T	C
Paper: Advanced Computer Architecture	4	0	4	

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: Computer architecture is the science and art of selecting and interconnecting hardware components to create a computer that meets functional, performance and cost goals. This course qualitatively and quantitatively examines computer design tradeoffs.

Unit 1

Parallel computer models[T1] [T2]:
The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivector and SIMD computers. (4 lectures)

Program and network properties [T1] [T2]: Conditions of parallelism, Data and resource Dependences, Hardware and software Parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms. (6 lectures)

Unit 2

System Interconnect Architectures [T1] [T2]:
Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network. (5 lectures)

Advanced processors [T1]: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors. (5 lectures)

Unit 3

Pipelining[T1] [T2]:
Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines. (6 lectures)

Memory Hierarchy Design[T1] [T2]:
Cache basics & cache performance, reducing miss rate and miss penalty, multilevel cache hierarchies, main memory organizations, design of memory hierarchies. (4 lectures)

Unit 4

Multiprocessor architectures[T1] [T2]:
Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenges of directory protocols, memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization. (6 lectures)

Scalable point – point interfaces[T1] [T2]:
Alpha364 and HT protocols, high performance signaling layer. (2 lectures)

Enterprise Memory subsystem Architecture[T1] [T2]:
Enterprise RAS Feature set: Machine check, hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system. (2 lectures)

Text Books:

[T1] Kai Hwang, "Advanced computer architecture"; TMH. 2000

[T2] D. A. Patterson and J. L. Hennessey, "Computer organization and design", Morgan Kaufmann, 2nd Ed. 2002.

Reference Books:

[R1] J. P. Hayes, "computer Architecture and organization"; MGH. 1998.

[R2] Harvey G. Cragon," Memory System and Pipelined processors" Narosa Publication. 1998.

[R3] V. Rajaranam & C. S. R. Murthy, "Parallel computer"; PHI. 2002

[R4] R.K.Ghose, Rajan Moona & Phalguni Gupta, "Foundation of Parallel Processing", Narosa Publications, 2003.

[R5] Kai Hwang and Zu, "Scalable Parallel Computers Architecture", MGH. 2001.

[R6] Stalling W, "Computer Organisation & Architecture", PHI. 2000.

[R7] D.Sima, T.Fountain, P.Kasuk, "Advanced Computer Architecture-A Design space Approach", Addison Wesley,1997.

[R8] M.J Flynn, "Computer Architecture, Pipelined and Parallel Processor Design"; Narosa Publishing, 1998.

[R9] D. A. Patterson, J. L. Hennessy, "Computer Architecture: A quantitative approach"; Morgan Kauffmann feb, 2002.

[R10] Hwan and Briggs, "Computer Architecture and Parallel Processing"; MGH. 1999.

Code No: ITV-651		**L**	**P**	**C**
Lab : DSD Lab	**-**	**2**	**2**	

Experiment of the lab will be based on Digital System Design with Verilog.

Code No. : ITV-653		**L**	**P**	**C**
Lab : Digital IC Design Lab	**-**	**2**	**2**	

Experiment of the lab will be based on MOS Circuit Design.

Code No: ITV-655		**L**	**P**	**C**
Lab : AAD Lab	**-**	**2**	**2**	

Experiment of the lab will be based on Algorithm Analysis and Design.

Paper Code: ITV-602	L	T	C
Paper: Analog VLSI Design	4	-	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The objective of this course is to become familiar with practical design aspects of analog integrated Circuits in CMOS Technology. Emphasis on the design of differential amplifier, current mirrors, operational amplifiers, linear operational transconductance amplifiers converters and comparators is given in this course. Students learn how to size all transistors in an analog integrated circuit in order to meet design specifications: matching, slew rate, bandwidth, DC offset, power dissipation, minimum supply voltage.

Unit 1

Small Signal & large signal Models of MOS & BJT transistor. Analog MOS Process (Double Poly Process) . (2 lectures)

MOS & BJT Transistor Amplifiers [T1] : Single transistor Amplifiers stages: Common Emitter, Common base, Common Collector, Common Drain, Common Gate & Common Source Amplifiers

Multiple Transistor Amplifier stages: CC-CE, CC-CC, & Darlington configuration, Cascode configuration, Active Cascode. Differential Amplifiers: Differential pair & DC transfer characteristics. (6 lectures)

Unit 2

Current Mirrors, Active Loads & References [T1]

Current Mirrors: Simple current mirror, Cascode current mirrors Widlar current mirror, Wilson Current mirror, etc. Active loads, Voltage & current references. Analysis of Differential Amplifier with active load, supply and temperature independent biasing techniques, Frequency Response. (8 lectures)

Unit 3

Operational Amplifier [T1]: Applications of operational Amplifier, theory and Design; Definition of Performance Characteristics; Design of two stage MOS Operational Amplifier, two stage MOS operational Amplifier with cascodes, MOS telescopic-cascode operational amplifiers, MOS Folded-cascode operational amplifiers, Bipolar operational amplifiers. Frequency response & compensation. (10 lectures)

Unit 4

Nonlinear Analog Circuits [T1] [T2]:

Analysis of four quadrant and variable Tran conductance multiplier, Voltage controlled oscillator, Comparators, Analog Buffers, Source Follower and Other Structures. Phase Locked Techniques; Phase Locked Loops (PLL), closed loop analysis of PLL. Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters. (8 lectures)

OTA & Switched Capacitor filters [T1]

OTA Amplifiers, Switched Capacitor Circuits and Switched Capacitor Filters. (4 lectures)

Text books:

[T1] Paul B Gray and Robert G Meyer, "Analysis and Design of Analog Integrated Circuits".

[T2] Behzad Razavi, "Principles of data conversion system design", S.Chand and company Ltd, 2000. John Wiley

Reference Books:

[R1] D. A. Johns and Martin, Analog Integrated Circuit Design, John Wiley, 1997.

[R2] Gregorian and G C Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley, 1986.

[R3] R L Geiger, P E Allen and N R Strader, VLSI Design Techniques for Analog & Digital Circuits, McGraw Hill, 1990.

[R4] Gray and Meyer," Analysis and Design of Analog IC ", Wiley international,1996.

[R5] Gray, Wooley, Brodersen, "Analog MOS Integrated circuits", IEEE press, 1989.

[R5] Kenneth R. Laker, Willy M.C. Sensen, " Design of Analog Integrated circuits and systems", McGraw Hill, 1994.

Paper Code: ITV –604	L	T	C
Paper: Advance VLSI Design	4	0	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: Introduce students to trade-offs in modern MOS technologies, and their impact on computer architecture and microarchitecture. Introduce students to the CAD tools needed to manage the complexity of VLSI designs.

Unit 1

VLSI System Design methodology [T1]: Structure Design, Strategy, Hierarchy, Regularity, Modularity, Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design. (6 lectures)

Unit 2

Chip Design Methods[T1]: Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System Design capture tools: HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification. (8 lectures)

Data Path Sub System Design[T1]: Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations. (5 lectures)

Unit 3

Subsystem Design[T1]: SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays. (4 lectures)

Control Unit Design [T1]: Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation. Special purpose Subsystems, Packaging, power distribution, I/O, Clock, Transconductance amplifier, follower integrated circuits. (8 lectures)

Unit 4

Design Economics[T1]: Nonrecurring and recurring engineering Costs, Fixed Costs, Schedule, Person power**.** (1 lectures)

VLSI System Testing & Verification[T1]: Introduction, A walk through the Test Process, Reliability, Logic Verification Principles, Silicon Debug Principles, Manufacturing Test Principles, Design for Testability, Boundary Scan**. V**LSI Applications like RISC microcontroller, ATM Switch. (9 lectures)

Text Books:

[T1] Neil H.E. Weste, Davir Harris, "CMOS VLSI Design: A Circuits and system perspectives" Pearson Education 3rd Edition, 2004.

Reference Books:

[R1] Wayne, Walf, "Modern VLSI design: System on Silicon" Pearson Education, 2nd Edition, 1998

[R2] Pucknull, "Basic VLSI Design" PHI 3rd Edition

Paper Code: ITV-606	L	T	C	
Paper: Computational Technique		4	-	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The development of fast, efficient and inexpensive computers has significantly increased the range of engineering problems that can be solved reliably. Computational techniques use computers to solve problems by step-wise, repeated and iterative solution methods, which would otherwise be tedious or unsolvable by hand-calculations. This course is designed to give an overview of computational techniques of interest to process engineer.

Unit 1

Functions of a complex variable: [T1]

Limit, continuity and differentiability. Analytical functions, Cauchy-Riemann equations, Cauchy integral theorem, singularities Taylor's and Laurent Series, Conformal mapping. (6 lectures)

Roots Finding for Non Linear equation: T2]

Functions and Polynomials, Zeros of a function, Roots of a Nonlinear equation, Bracketing, Bisection and Newton-Raphson Methods, Polynomial fits. (6 lectures)

Unit 2

Interpolation: [T3]

Nwton's (Newton-Gregory) Forwarded Difference (FD) Formula and Backward Difference (BD) Formula. Lagrange's Divided differences and Newton's Divided Formula. (5 lectures)

Numerical Integration: [T3]

Evaluation of Integrals, Elementary Analytical Methods, Trapezoidal and Simpson's Rules, Gaussian Quadrature, and orthogonal polynomials, Multidimensional Integrals, Numerical differentiation and Estimation of errors. (8 lectures)

Unit 3

Numerical Solution of Linear equation: [T3]

Vectors and Matrices, Solutions of linear algebraic equations by direct and iterative methods, Gaussian elimination, LU, Cholesky and singular value decompositions, Matrix diagonalization methods. (8 lectures)

Unit 4

Numerical Methods for ordinary differential equation: [T3]

Solution of initial-value problems of systems of ODEs. Single step and multistep methods, convergence. Finite difference methods for the solution of two-point boundary-value problem. (7 lectures)

Text Books:

[T1] Murray R Spiegel, "Theory and Problems of Complex Variables", Schaum's Outline Series, New York.

[T2] Conte, S. D. de Boore, C. "Elementary Numericla Analysis" McGraw Hill

[T3] Pradip Niyogi, "Numerical Analysis & Algorithms", TMH, 2003

References Books:

[R1] Kreyszig, E, "Advanced Engineering Mathematics", John Wiley & Sons, 8th Edition, 2002

[R2] Radhey S Gupta, "Elements of Numerical Analysis", Macmillan

[R3] Brian Bradie, "A Friendly Introduction to Numericla Analysis" Pearson.

[R4] Chapra, S. C, Canale R P, "Numerical Methods for Engineers", 3rd Ed., McGraw-Hill 1998

[R5] Curtis F. Gerald, Patrick O. Wheatley, "Applied Numerical Analysis", Pearson 7th Edition.

Paper Code: ITV-608	L	T	C
Paper: Low Power VLSI Design	4	-	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The goal of the course is to learn principles of design, analysis, modeling and optimization of Low Power VLSI. In this course you will study the approaches for power consumption estimation and different methods to reduce the power consumption, low power architectures and algorithmic level analysis for low power optimization.

Unit 1

Introduction[T1] [T2]: Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices. (3 lectures)

Device & Technology Impact on Low Power [R1]: Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation. Power estimation Techniques. (4 lectures)

Unit 2

Simulation Power analysis [T1]: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. (10 lectures)

Unit 3

Low Power Techniques[T1] : Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic. (6 lectures)

Low power Architecture & Systems[T1] Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. (6 lectures)

Unit 4

Low power Clock Distribution[T2]: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. (3 lectures)

Algorithm & architectural level methodologies[T1] : Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis. (4 lectures)

Text Books:

[T1] Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002

[T2] Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997

Reference Books:

[R1] Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.

Paper Code: ITV-610	L	T	C
Paper: VLSI Test & Testability	4	-	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The objective of the course is to introduce students to VLSI testing, test process and automatic test equipment, test economics and product quality, fault modeling, logic and fault simulation, testability measures, combinational and sequential circuit test generation, memory test, analog test, delay test, IDDQ test, design for testability, built-in self-test, boundary scan, analog test bus, system test and core test.

Unit 1

Introduction[T1]: The need for testing, the problems of digital and analog testing, Design for test, Software testing. (2 lectures)
Faults in Digital circuits[T1]: General introduction, Controllability and Observability.. Fault models - Stuck-at faults, Bridging faults, intermittent faults. (8 lectures)

Unit 2
Digital test pattern generation[T1]: Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D-algorithm, Developments following Roth's D-algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits, Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing. (10 lectures)

Unit 3
Signatures and self test[T1]: Input compression Output compression Arithmetic, Reed-Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients, Spectral coefficients, Coefficient test signatures, Signature analysis and Online self test. (6 lectures)

Unit 4
Testability Techniques[T1]: Partitioning and ad hoc methods and Scan-path testing, Boundary scan and IEEE standard 1149.1, Offline BIST, Hardware description languages and test. (4 lectures)
Testing of Analog and Digital circuits[T1]: Testing techniques for Filters, A/D Converters, RAM, Programmable logic devices and DSP. (5 lectures)

Text Books:
[T1] VLSI Testing: digital and mixed analogue digital techniques. Stanley L. Hurst Pub:Inspec/IEE ,1999.

Reference Books:
[R1] M L Bushnell and V D Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits'", Springer, 2005.

Paper Code : ITR – 604	L	T	C
Paper: Embedded System Design using 8051		4 -	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The objective of the course is to teach students all aspects of the design and development of an embedded system, including hardware and embedded software development.

Unit 1[T1]

Introduction to Embedded Realtime Systems: Fundamental components of ESD, Preprocessing, Compiling, cross compiling, Linking, Locating, compiler driver, Linker script, Program segments, Type of memory, Memory Management in Embedded real-time systems, Interrupt and ISR. (6 lectures)

Unit 2[T1]

Introduction to Real-time theory: Scheduling theory, Rate Monotonic Scheduling, Utilization bound theorem, RTOS, Task Management, Task management, Race condition, Priority inversion, ISRs and scheduling, Inter-Task communication, Timers. (6 lectures)

Unit 3[T2]

Microcontrollers: Role of processor selection in Embedded System (microprocessor vs microcontroller), 8051 microcontroller: architecture, assembly language programming, instruction set, addressing mode, logical operation, arithmetic operation, interrupt handling, Timing subroutines. (10 lectures)

Unit 4 [T1] [T2]

Serial data communication, RS-232, USB, I^2C, Interfacing with ADC & sensors, Interfacing with DAC, Interfacing with external ROM, Interfacing with 8255 IEEE 1149.1 (JTAG) testability: Boundary Scan Architecture . (10 lectures)

Text Books:

[T1] Sriram V Iyer and Pankaj Gupta, "Embedded Real-time Systems Programming", TMH 2006.

[T2] Mazidi and Mazidi, "The 8051 Microcontroller", PHI, 2006

Reference Books:

[R1] Embedded System by Raj Kamal, TMH, 2004

[R2] The 8051 Microcontroller by Kennth J. Ayala, Thomson DelMar Learning, 2006

[R3] Microcontrollers by Deshmukh, TMH, 2006

[R4] 8051 Microcontroller & Embedded systems by Rajiv Kapadia, Jaico, 2006

[R5] Computer as components by wayne wolf, Harcourt India Pvt. Ltd, 2002

[R6] Real time System and Analysis by Philip A. Laplante, Wiley, 2006

[R7] Microcontrollers and microcomputers by F. M. Cady, Oxford Press, 2006

[R8] An Embedded Software Primer by David E. Simon, Pearson Education, 2005

[R9] Designing Embedded Hardware by John Catsoulis, O'reily 2005

[R10] Real time System & Software by Alan c. Shaw, Wiley, 2005

Paper Code: ITV–612	L	T	C
Paper: Designing with ASICS	4	-	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: To introduce students to the process of designing application specific hardware implementations of algorithms for ASICs. Students will work with commercial computer aided design tools to synthesize designs described in hardware description languages.

Unit 1

Types of ASICs[T1] – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers. (6 lectures)

Unit 2

ASIC Library design[T1]: Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis. (10 lectures)

Unit 3[T1]

Half gate ASIC, Low level design entry: Schematic entry – low level design languages – PLA tools – EDIF – An overview of VHDL and Verilog. (10 lectures)

Unit 4[T1]

Logic synthesis in Verilog and VHDL simulation.
ASIC Construction – Floor planning & placement – Routing. (10 lectures)

Text Books:

[T1] J.S. Smith, "Application specific Integrated Circuits", Addison Wesley, 1997.

Reference Books:

[R1] Bakoglu, H. B. Circuits, Interconnections, and Packaging for VLSI. Reading, MA: Addison-Wesley, 1990.

[R2] Einspruch N. G., and J. L. Hilbert (Eds.). Application Specific Integrated Circuit (ASIC) Technology, CA: Academic Press, 1991.

Paper Code: ITR – 610	L	T	C
Paper: Digital Signal Processing	4	-	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The course introduces fundamental concepts, algorithms and applications of DSP. The course starts from the fundamental description of how signals can be represented as digital waveforms to how systems may be modeled as digital filters. Then analyze discrete time systems using time domain, frequency domain and z-domain mathematics. Design and implement FIR and IIR digital filters for real world applications in digital audio, acoustics and telecommunication.

Unit 1

Introduction[T1]: signals and signal Processing, characterization & classification of signals, typical Signal Processing operations, example of typical Signals, typical Signals Processing applications. (2 lectures)

Time Domain Representation of Signals & Systems[T1] [T2]

Discrete Time Signals, Operations on Sequences, Linear shift-invariant systems, Stability and Causality, Linear constant coefficient difference equations, Frequency domain representation of discrete-time systems, symmetry properties of the Fourier transform, Sampling of continuous-time systems. (6 lectures)

Unit 2

Transforms[T1] [T2]

Z-transforms, Inverse Z-transform, properties of Z-transform, & its applications in system analysis & design. Discrete Fourier Transform (DFT) & its properties, computation of the DFT of real sequences, Linear Convolution using the DFT. (5 lectures)

Digital Filter Structure[T1] [T2]

Block Diagram representation, Signal Flow Graph Representation, Equivalent Structures, Basic FIR Digital Filter Structures: Direct forms, Transposed forms, Cascaded forms, Poly phase realization and Linear phase FIR structures. Basic IIR Filter Structures: Direct forms, Transposed forms, Cascaded realizations and Parallel realizations. All pass filters, Digital Sine-Cosine Generator. (8 lectures)

Unit 3

Digital Filter Design [T1] [T2]

Design of IIR Digital filters from analog filters, Properties of FIR digital filters, Desgin of FIR filters using Windows, Computer aided design of FIR filters, Comparison of IIR and FIR digital filters. (10 lectures)

Unit 4

Computation of Discrete Fourier Transform [T1] [T2]

Complexity of the DFT computation by direct method, Goertzel algorithm, Decimation –in-time FFT algorithms, Decimation-in frequency FFT algorithms. (7 lectures)

Text Books:

[T1] Alan V. Oppenheim & Ronald W. Schafer, " Digital Signal Processing" PHI, 2002.

[T2] Sanjit K. Mitra, " Digital Signal Processing: A computer based approach" TMH, 2nd Edition, 2003.

Reference Books:

[R1] Chi-Tsong Chen, " Digital Signal Processing, Spectral Computation and Filter Design" Oxford University Press, 2001.

[R2] Monson H. Hayes, " Schaum's Outline of Digital Signal Processing", Mcgraw Hill, 1999.

[R3] Richard W. Hammming, "Digital Filters", Dover Pubns, 1998.

[R4] Lars Wanhammar, " DSP Integrated Circuits", Academic Press, First edition, 1999.

[R5] Simon S. Haykin, " Adaptive Filter Theory, " Prentice Hall, 3rd Edition.

Paper Code: ITR – 612	L	T	C
Paper: Real Time Systems and Software	4	-	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The aim of the course is that the students learn to validate formal specifications, in particular of real-time systems, with the aid of software tools for the verification and analysis. In addition, they should learn to understand the main underlying theoretical and practical problems.

Unit 1

Introduction[T1]: Real-time Versus Conventional Software, Computer Hardware for Monitoring and Control, Software Engineering Issues. (3 lectures)

Software Architectures[T1]: Process and State-based Systems model, Periodic and Sporadic Process, Cyclic Executives, CE definitions and Properties, Foreground-Background Organizations, Standard OS and Concurrency, Systems Objects and Object-Oriented Structures, Abstract Data Types, General Object Classes. (6 lectures)

Unit 2

Requirements and Design Specifications[T1]: Classification of Notations, Data Flow Diagrams, Tabular Languages, State Machine, Communicating Real Time State Machine- Basic features, Timing and clocks, Semantics Tools and Extensions, State charts-Concepts and Graphical Syntax, Semantics and Tools. (4 lectures)

Declarative Specifications[T1]: Regular Expressions and Extensions, Traditional Logics-Propositional Logic, Predicates, Temporal logic, Real time Logic. (2 lectures)

Deterministic Scheduling[T1: Assumptions and Candidate Algorithms, Basic RM and EDF Results, Process Interactions-Priority Inversion and Inheritance. (4 lectures)

Unit 3

Execution Time Prediction[T1]: Measurement of Software by software, Program Analysis with Timing Schema, Schema Concepts, Basic Blocks, Statements and Control, Schema Practice, Prediction by optimization, System Interference and Architectural Complexities

Timer Application, Prosperities of Real and ideal clocks, Clock Servers – Lamport's Logical clocks, Monotonic Clock service, A software Clock server, Clock Synchronization- Centralized Synchronization, Distributed Synchronization. (10 lectures)

Unit 4

Programming Languages[T1]: Real Time Language Features, Ada-Core Language, Annex Mechanism for Real Time Programming, Ada and Software Fault Tolerance, Java and Real-time Extensions, CSP and Occam. (4 lectures)

Operating Systemsv[T1]: Real Time Functions and Services, OS Architectures-Real Time UNIX and POSIX, Issues in Task management- Processes and Threads, Scheduling, Synchronization and communication. (6 lectures)

Text Book:

[T1] Real – Time Systems and software by Alan C. Shaw ; John Wiley & Sons Inc, 2001

Reference Books:

[R1] Jane W.S. Liu, Real-Time Systems, Prentice Hall, 2000.

Paper Code: ITV – 614	L	T	C
Paper: Microwave & Optoelectronic Devices	4	-	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: To acquaint the student with the devices that are used in microwave and optoelectronics systems and the circuits that are used to interconnect them. The design and functioning of these devices and circuits are explained.

Unit 1

Introduction[T1] [T2]: Microwave frequencies, microwave transistor, microwave field effect transistor, tunnel diode, backward diode, and MIS tunnel diode, Transferred electron devices-Gunn Diode. (4 lectures)
Avalanche Transit Time Devices[T1] [T2]:: IMPATT Diode, BARRITT Diode, DOVETT Diode, and TRAPATT Diode. (4 lectures)

Unit 2

Microwave Integrated Circuit[T1] [T2]:: Introduction, Circuit Forms, Transmission lines for MICs, Lumped Elements for MICs, Material for MICs: Substrate, Conductor, dielectric and resistive Materials, Fabrication techniques, Typical example of fabrication, Hybrid fabrication. (6 lectures)
Microwave tubes[T1] [T2]:: Klystron, Reflex Klystron and Magnetron, Traveling wave tubes, microwave detection diodes, application of microwave. (4 lectures)

Unit 3

Introduction of optoelectronic devices[T3]: Photovoltaic devices, Solar Radiation, PN-Homojunction solar cells, Antireflection coatings, Ideal conversion efficiency, Spectral response, I-V Characteristics, Temperature and radiation effects, Heterojunction solar cells, Schottky barrier solar cell, Thin film and amorphous silicon solar cell. (10 lectures)

Unit 4

Solar arrays Display devices[T3]: Characterization of displays, drawbacks of cathode ray tube, Flat panel display: Electro luminescence displays (Powder and thin films), Plasma display, LCD, Electronchromic display and electrophoretic display. (8 lectures)

Text Books:

[T1] Microwave Devices and Circuits by S. Y. Liao, PHI, 1980.

[T2] Microelectronic Devices by E. S . Yang, MGH, 1988

[T3] Optoelectronics : An introduction by J. Wilson & JFB Hawkers, PHI, 1993.

Reference Books:

[R1] Physics of Semiconductor Devices by S M Sze, Willy Eastern Pub., 1981

[R2] Microwave Engineering and application by O.P. Gandhi, Maxwell Macmillan Pub., 1984

[R3] Topic in applied physics – Vol 40 by J.I. Pankove, Springer Verlag.

[R4] Semiconductor Devices and Integrated Electronics by A. G. Milness, CBS Pub.

Paper Code: ITR – 620	L	T	C
Paper: Neural Network	4	-	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The objective of the course is to introduce basic architecture of mobile and cellular services starting from 1G through to 2G(GSM). The prerequisites are Data communication, Antennas and wave propagation.

Unit 1[T1]

Biological analogy, Architecture classification, Neural Models, Learning Paradigm and Rule, single unit mapping and the perception. (6 lectures)

Unit 2[T1]

Feed forward networks – Review of optimization methods, back propagation, variation on Back propagation, FFANN mapping capability, properties of FFANN's Generalization. (8 lectures)

Unit 3[T1]

Recurrent Networks – Symmetric hopfield networks and associative memory, Boltzmann machine, Adaptive Resonance Networks. (8 lectures)

Unit4[T1]

PCA, SOM, LVQ, Adaptive Resonance Networks. Hopfield Networks, Associative Memories, RBF Networks. (6 lectures)

Applications of Artificial Neural Networks: Regression, applications to function approximation, Classification, Blind Source Separation. (4 lectures)

Text Book:

[T1] Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall International, New Jersey, 1999.

Reference Books:

[R1] Anderson J.A., "An Introduction to Neural Networks", PHI, 1999.

[R2] Hertz J, Krogh A, R.G. Palmer, "Introduction to the Theory of Neural Computation",

Addison-Wesley, California, 1991.

[R3] Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications and Programming Techniques", Addison-Wesley, Reading, Mass, (1992).

[R4] Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge, MA, 1996.

[R5] Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York, 1998.

[R6] Anderson J.A., E. Rosenfield, "Neurocomputing: Foundatiions of Research, MIT Press, Cambridge, MA, 1988

[R7] Patterson D.W., "Artificial Neural Networks: Theory and Applications", Prentice Hall, Singapore, 1995.

[R8] Vapnik V.N., "Statistical Learning Theory: Inference from Small Samples", John Wiley, 1998.

Code No : ITV - 616		**L**	**T**	**C**
Subject: Project Work	**4**	**-**	**4**	

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format. The student will have to present the progress of the work through seminars and progress report. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

Code No: ITV-652	**L**	**P**	**C**
Lab: AVDA	**-**	**2**	**3**

The experiments will be based on the following papers:
Analog VLSI Design.

Code No: ITV-654	**L**	**P**	**C**
Lab: Electives Lab	**-**	**2**	**3**

The experiments will be based on the elective papers if Lab is required.

Paper Code: ITV-701	L	T	C
Paper: Algorithm for VLSI Design Automation	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The goal of course is to study the Basic Algorithms used in Physical Design of VLSI Circuits, study of the algorithms to convert circuit description into geometric description and comparison of algorithms which perform same tasks. Learning about the physical design automation techniques used in the simulation / Synthesis (Tools) systems

Unit 1

VLSI automation Algorithms[T1]: General Graph theory and basic VLSI algorithms. (4 lectures)
Partitioning: problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing & evolution, other partitioning algorithms. (4 lectures)

Unit 2
Placement, floor planning & pin assignment[T1]: problem formulation, simulation base placement algorithms, other placement algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design. General & channel pin assignment. (8 lectures)

Unit 3
Global Routing[T1]: Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, ILP based approaches. (6 lectures)
Detailed routing[T1]: problem formulation, classification of routing algorithms, single layer routing algorithms, two layer channel routing algorithms, three layer channel routing algorithms, and switchbox routing algorithms. (6 lectures)

Unit 4
Over the cell routing & via minimization[T1]: two layers over the cell routers constrained & unconstrained via minimization. (6 lectures)
Compaction[T1]: problem formulation, one-dimensional compaction, two dimension based compaction, hierarchical compaction. (4 lectures)

Text Books:

[T1] Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition, 2005.

References Books:

[R1] Christophn Meinel & Thorsten Theobold, "Algorithm and Data Structures for VLSI Design", KAP, 2002.

[R2] Rolf Drechsheler : "Evolutionary Algorithm for VLSI", Second edition, 2002

[R3] Trimburger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

Paper Code: ITV - 703	L	T	C
Paper: Process, Devices & Circuit Simulation	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: To understand and appreciate the underlying physics and principles involved in silicon processing and device characterization. To relate theory on semiconductor processing and device physics to practical technology development and device design considerations. To get familiarized with the use of TCAD tools as a design aid in process and device simulation.

Unit 1[T1]

Introduction, Main data structure & program organization, Geometrical manipulations, Ion implantation. . (6 lectures)

Unit 2 [T1]

A novel measurement technique for 2D implanted ion distributions, Introduction to partial differential equation solver. (10 lectures)

Unit 3 [T1]

The merged multi grid method, Isothermal device modeling & simulation. . (8 lectures)

Unit 4 [T1]

Non-Isothermal device modeling & simulation, hydrodynamic device modeling & simulation. (10 lectures)

Text Books:

[T1] Circuit, Device and Process Simulation: Mathematical and Numerical Aspects by Graham F. Carey (Editor), W. B. Richardson, C. S. Reed, B. Mulvaney, John Wiley & Sons; 1st edition. 1996.

Reference Books:

[R1] Process and Device Simulation for MOS-VLSI Circuits, edited by P. Antognetti, D.A. Antoniadis , Robert W. Dutton, W.G. Oldham, Kluwer Academic Publisher, 2000.

Paper Code No : ITV - 705	L	T	C
Paper : Nano Technology	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The course covers technologies used to design, realise and analyse micro and nano-scale devices, materials and systems, coupled with general and technology management.

Unit 1[T1]

Introduction to nanoscale systems, Length energy and time scales, Top down approach to Nano lithography, Spatial resolution of optical, deep ultraviolet, X-ray, electron beam and ion beam lithography. (8 lectures)

Unit 2[T1]

Single electron transistors, coulomb blockade effects in ultra small metallic tunnel junctions .

Quantum Mechanics: Quantum confinement of electrons in semiconductor nano structures, Two dimensional confinement (Quantum wells), Band gap engineering, Epitaxial, Landaeur – Buttiker formalism for conduction in confined geometries, One dimensional confinement (10 lectures)

Unit 3[T1]

Quantum point contacts, quantum dots and Bottom up approach, Introduction to quantum methods for information processing. (5 lectures)

Molecular Techniques: Molecular Electronics, Chemical self assembly, carbon nano tubes, Self assembled mono layers. (4 lectures)

Unit 4 [T1]

Electromechanical techniques, Applications in biological and chemical detection, Atomic scale characterization techniques, scanning tunneling microscopy, atomic force microscopy. (8 lectures)

Text Books:

[T1] Beenaker and Van Houten "Quantum Transport in Semiconductor Nanostructures in Solid state Physics" Ehernreich and Turnbell, Academic press, 1991

Reference Books:

[R1] David Ferry " Transport in Nano structures" Cambridge University press 2000

[R2] Y. Imry " Introduction to Mesoscopic Physics, Oxford University press 1997

[R3] S. Dutta " Electron Transport in Mesoscopic systems" Cambridge University press 1995

[R4] H. Grabert and M. Devoret "Single charge Tunneling" Plenum press 1992

Paper Code: ITV - 707	L	T	C
Paper: Hardware-Software Co-design	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The objective of the course is to present techniques for the concurrent design, or co-design, of hardware and software. Special emphasis will be placed upon methods used for the development of embedded systems that are dedicated to specific applications and consist of tightly coupled hardware and software components.

Unit 1

Introduction [T1]: Motivation hardware & software co-design, system design consideration, research scope & overviews. Hardware Software back ground: Embedded systems, models of design representation, the virtual machine hierarchy, the performance3 modeling, Hardware Software development. (4 lectures)

Unit 2

Hardware Software co-design research[T1]: An informal view of co-design, Hardware Software tradeoffs, crosses fertilization, typical co-design process, co-design environments, limitation of existing approaches, ADEPT modeling environment. **Co-**design concepts: Functions, functional decomposition, virtual machines, Hardware Software partitioning, Hardware Software partitions, Hardware Software alterations, Hardware Software trade offs, co-design. (10 lectures)

Unit 3

Methodology for co-design[T1]: Amount of unification, general consideration & basic philosophies, a framework for co-design. Unified representation for Hardware & Software : Benefits of unified representation, modeling concepts. An abstract Hardware & Software model : Requirement & applications of the models, models of Hardware Software system, an abstract Hardware Software models, generality of the model. (10 lectures)

Unit 4

Performance evaluation[T1]: Application of t he abstract Hardware & Software model, examples of performance evaluation .Object oriented techniques in hardware design: Motivation for object oriented technique, data types, modeling hardware components as classes, designing specialized components, data decomposition, Processor example. (10 lectures)

Text Books:

[T1] Sanjaya Kumar, James H. Ayler "The Co-design of Embedded Systems: A Unified Hardware Software Representation", Kluwer Academic Publisher, 2002.

Reference Books:

[R1] H. Kopetz, Real-time Systems, Kluwer, 1997.

[R2] R. Gupta, Co-synthesis of Hardware and Software for Embedded Systems, Kluwer 1995.

[R3] S. Allworth, Introduction to Real-time Software Design, Springer-Verlag, 1984.

[R4] Peter Marwedel, G. Goosens, Code Generation for Embedded Processors, Kluwer Academic Publishers, 1995.

Paper Code: ITV - 709	L	T	C
Paper: Genetic Algorithms for VLSI Design	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: To familiarize students with genetic and evolutionary computation techniques and to enable them to read the literature and solve practical problems of VLSI Physical design like partitioning, floorplanning and placement.

Unit 1

Introduction [T1]:

Introduction to GA, Simple GA, Steady state algorithm, Genetic Operators, GA for VLSI Design, Layout and Test Automation. (6 lectures)

Unit 2

Partitioning and Cell Placement and Routing [T1]:

Partitioning algorithms, Circuit Partitioning by Genetic Algorithms, Hybrid Gas for radio cut partitioning, Standard and Macro cell placement, Steiner problem in graph, macro cell global routing. (8 lectures)

Unit 3

FPGA Technology mapping and automatic test generation [T1]:

Circuit segmentation and FPGA Mapping, Circuit segmentation for pseudo exhaustive testing, Test generation in GA framework, Genetic test generator hybrids, Use of Finite State Machine Sequences and dynamic test sequence compaction. (10 lectures)

Unit 4

Peak Power estimation and parallel implementations [T1]:

Problem description, application of GA to Peak Power estimation, Peak sustainable Power estimation, Wolverines: Standard cell placement on a network of workstations, Parallel GAs for automatic test generation, Problem encoding, fitness function, Genetic Algorithms vs. Conventional Algorithms. (10 lectures)

Text Book:

[T1] Pinaki Mazumder, Elizabeth M. Rudnick, "Genetic algorithms for VLSI Design, Layout and Test Automation " Pearson Education, 2007

Reference Books:

[R1] Melanle Mitchell, "An introduction to genetic algorithms", Prentice Hall India, 2002.

[R2] Michael D. Vose, "The simple genetic algorithm foundations and theory, Prentice Hall India, 1999.

Paper Code: ITV - 711	L	T	C
Paper: CMOS RF Circuit Design	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: Understand Modern RFIC Architectures. Describe RF circuit parameters and terminology. State the effects of parasitic on circuit performance at RF. Use graphical design techniques and the Smith Chart. Match impedances and perform transformations. Understand key active circuit design issues.

Unit 1

Introduction [T1]: RF design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion. (6 lectures)

Unit 2

RF Modulation [T1]:

Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures. Direct conversion and two-step transmitters. (6 lectures)

RF Testing [T1]:

RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers. (4 lectures)

Unit 3

BJT and MOSFET Behavior at RF Frequencies [T1]:

BJT and MOSFET behavior at RF frequencies, Modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation . (6 lectures)

Unit 4

RF Circuits Design [T1]:

Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. (5 lectures)

Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. (4 lectures)

Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters. (5 lectures)

Text Book:

[T1] Thomas H. Lee "Design of CMOS RF Integrated Circuits" Cambridge University press 1998.

Reference Books:

[R1] B. Razavi "RF Microelectronics" PHI, 1998.

[R2] R. Jacob Baker, H.W. Li, D.E. Boyce " CMOS Circiut Design, layout and Simulation" PHI,1998.

[R3] Y.P. Tsividis "Mixed Analog and Digital Devices and Technology", TMH 1996

Paper Code No : ITV - 713		L	T	C
Paper : Cryptology and Crypto chip Design	4	0	4	

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The objective of the course consists is twofold:
•Understand the mathematical properties and techniques for cryptography.
•Understand the algorithms of cryptography and estimate the strength of the cryptographic functions.

Unit 1
Basic concepts [T1]:
Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS,, Targets: Hardware, Software, Data communication procedures. (3 lectures)
Threats to Security:
Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security. (4 lectures)
Unit 2
Encryptions Techniques[T1]:
Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management. (5 lectures)
Message Authentication and Hash Algorithm:
Authentication requirements and functions secure Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service. (5 lectures)
Unit 3
Firewalls and Cyber laws[T1]:
Firewalls, Design Principles, Trusted systems, IT act and cyber laws, Virtual private network. (4 lectures)
Future Threats to Network:
Recent attacks on networks, Case study (3 lectures)
Unit 4
Applications[T1]:
AES algorithm. Crypto chip design: Implementation of DES, IDEA AES algorithm, Development of digital signature chip using RSA algorithm. (10 lectures)

Text Books:

[T1] William Stalling "Cryptography and Network Security" Pearson Education, 2005

References:

[R1] Charels P. Pfleeger "Security in Computing" Prentice Hall, 2006

[R2] Jeff Crume "Inside Internet Security" Addison Wesley, 2000.

Paper Code No : ITV – 715	**L**	**T**	**C**
Paper : MEMS and IC Integration	**4**	**0**	**4**

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: Introduction to Micro-world. Basic IC and micro-fabrication. Non IC-based micro machining. MEMS applications: micro sensors & micro actuators, micro system. Global activities around the world.

Unit 1 [T1] [T2]
Overview of CMOS process in IC fabrication, MEMS system-level design methodology. (6 lectures)

Unit 2 [T1] [T2]
Equivalent Circuit representation of MEMS, signal-conditioning circuits, and sensor noise calculation. (10 lectures)

Unit 3[T1] [T3] [T5]
Pressure sensors with embedded electronics(Analog/Mixed signal): Accelerometer with transducer, Gyroscope, RF MEMS switch with electronics. (10 lectures)

Unit 4 [T1] [T3] [T5]
Bolo meter design. RF MEMS, and Optical MEMS. (10 lectures)

Text Books:

[T1] Gregory T.A. Kovacs, Micromachined Transducers Sourecbook, The McGraw-Hill, Inc. 1998
[T2] Stephen D. Senturia, Microsystem Design, Kluar Publishers, 2001
[T3] Nadim Maluf, An Introduction to Microelectromechanical Systems Engineering, Artech House, 2000.
[T4] M.H. Bao, Micro Mechanical Transducers, Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000.
[T5] H. J. De Los Santos, Introduction to Microelectromechanical (MEM) Microwave Systems, Artech, 1999.

Reference Books

[R1] Masood Tabib-Azar, Microactuators, Kluwer, 1998.
[R2] Ljubisa Ristic, Editor, Sensor Technology and Devices, Artech House, 1994
[R3] D. S. Ballantine, et. al., Acoustic Wave Sensors, Academic Press, 1997
[R4] James M.Gere and Stephen P. Timoshenko, Mechanics of Materials, 2nd Edition, Brooks/Cole Engineering Division, 1984

Paper Code: ITV - 717	L	T	C
Paper: Computer aided VLSI Design	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: To understand the principles of hierarchical design of digital VLSI systems. To utilize CAD tools to explore design alternatives and enhance productivity. To experience the above goals through practical homework assignments implementing custom integrated circuits.

Unit 1 [T1]
Hardware description languages; Verifying behavior prior to system construction simulation and logic verification; Logic Synthesis PLA based synthesis and multilevel logic synthesis. (8 lectures)

Unit 2 [T1]
Logic optimization; Logic Simulation Compiled and event simulators; Relative advantages and disadvantages; Layout Algorithms Circuit partitioning, placement, and routing algorithms. (10 lectures)

Unit 3 [T1]
Design rule verification; Circuit Compaction; Circuit extraction and post-layout simulation; Automatic Test Program Generation. (8 lectures)

Unit 4 [T1]
Combinational testing D-Algorithm and PODEM algorithm; Scan-based testing of sequential circuits; Testability measures for circuits. (8 lectures)

Text Books:

[T1] "Algorithm and Data Structures for VLSI Design", Christophn Meinel & Throsten Theobold, 2002.

Reference Books:

[R1] "Evolutionary Algorithm for VLSI", Rolf Drechsheler ,

Paper Code: ITV - 719	L	T	C
Paper: Designing with AVR microcontroller	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

3. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
4. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

UNIT – I

Microcontroller architecture, The AVR RISC Microcontroller Architecture: AVR family architecture, Register File, Memory access and instruction Execution, I/O Memory, I/O Ports.

UNIT – II

AVR Instruction Set: Program and data addressing modes, Arithmetic & Logic Instruction, Program Control Instruction, Data Transfer Instruction

AVR Hardware Design Issues: Power source, Operating clock sources, Reset circuit

UNIT – III

Hardware & Software Interfacing with AVR: Lights & switches, Stack operation in AVR Processors, Implementing Combinational Logic, Connecting the AVR to the PC serial port, Expanding I/O, Interfacing analog to Digital converters and DAC, Interfacing with LED/LCD displays, Stepper motor interface with AVR.

UNIT – IV

Communication links for the AVR Processor: RS-232 Link, RS-422/423 link, SPI and microwave bus, IrDA Data link, CAN

AVR System Development tool: Code assembler, Code simulator, Evaluation boards, AVR emulator, Device Programmer

TEXT BOOKS:

1. Dhananjay V. Gadre, "Programming and Customizing the AVR Microcontroller", TMH 2003

Paper Code: ITV –721	L	T	C
Paper: Advanced Computational Methods	4	0	4

INSTRUCTIONS TO PAPER SETTERS: Maximum Marks : 60

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: Application of advanced computational methods for solving nonlinear problems in VLSI Design. Development and use of state-of-the-art mathematical and numerical algorithms including high-performance computing to develop the CAD Tools for design automation.

Unit 1

Solution of two or more nonlinear equations by iterative methods (Picard and Newton's methods) Spline interpolation, cubic splines, Chebyshev polynomials, Minimax approximation. (10 lectures) **[T1]**

Unit 2

Eigen values and vectors of a real symmetric matrix – Jacobi method. Eigen value problem for ordinary differential equations. (6 lectures) **[T2]**

Numerical solution of a parabolic equation. Explicit method, simple implicit method and Crank-Nicholson method. Stability. (6 lectures) **[T3]**

Unit 3

Numerical Solution of elliptic problems. Dirichlet and Neumann problems (Cartesian and Polar coordinates), Numerical solution of hyperbolic equations. Explicit method. Method of characteristics. Stability. (9 lectures) **[T4]**

Unit 4

The finite element method – Ritz, collocation and Galerkin methods. Boundary value problems for ordinary differential equations. Shape functions. Assembly of element equations. (9 lectures) **[T4]**

Text Books:

[T1] Niyogi, P. "Numerical Analysis and Algorithms", TMH, 2003.

[T2] Curtis F. Gerald, Patrick O. Wheatley, "Applied Numerical Analysis", Pearson 7th Edition.

[T3] Brian Bradie, "A Friendly Introduction to Numericla Analysis" Pearson.

[T4] Radhey S Gupta, "Elements of Numerical Analysis", Macmillan

Reference Books:

[R1] Jain, M. K., "Numerical Solution of Differential Equations", Wiley Eastern Ltd.

[R2] Smith G. D. "Numerical Solution of Partial Differential Equation", Oxford, 1965.

[R3] Chapra, S.C, Canale R P "Numerical Methods for Engineers" 3rd Ed., McGraw-Hill 1998.

[R4] Froberg, C. E., "Introduction to Numerical Analysis", Addison-Wesley Publishing Co.

[R5] Jain, M. K., Iyengar, S.R.K., and Jain, R.K., "Numerical Methods for Scientific and Engineering Computations", New Age International (P) Ltd, Publishers.

Paper Code: ITV - 723	**L**	**T**	**C**
Paper: Project Work	**4**	**0**	**4**

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format. The student will have to present the progress of the work through seminars and progress report. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format.

Paper Code: ITR –727	L	T	C
Paper: Digital Image Processing	4	0	4

INSTRUCTIONS TO PAPER SETTERS: **Maximum Marks : 60**

1. **Question No. 1 should be compulsory and cover the entire syllabus. This question should have objective or short answer type questions. It should be of 20 marks.**
2. **Apart from Question No. 1, rest of the paper shall consist of four units as per the syllabus. Every unit should have two questions. However, student may be asked to attempt only 1 question from each unit. Each question should be 10 marks**

Objective: The aim of this course is to provide students with a basic understanding of digital image processing techniques. The material will emphasize the fundamentals of image acquisition, representation, compression, and frequency and spatial domain transformations and applications.

Unit 1

Introduction And Digital Image Fundamentals [T2]:

The origins of Digital Image Processing, Examples of Fields that Use Digital Image Processing, Fundamentals Steps in Image Processing, Elements of Digital Image Processing Systems, Image Sampling and Quantization, Some basic relationships like Neighbors, Connectivity, Distance Measures between pixels, Linear and Non Linear Operations. (6 lectures)

Unit 2

Image Enhancement in the Spatial Domain [T1]:

Some basic Gray Level Transformations, Histogram Processing, Enhancement Using Arithmetic and Logic operations, Basics of Spatial Filters, Smoothening and Sharpening Spatial Filters, Combining Spatial Enhancement Methods. Image Enhancement in the Frequency Domain.

Introduction to Fourier Transform and the frequency Domain, Smoothing and Sharpening Frequency Domain Filters, Homomorphic Filtering. Image Restoration. (10 lectures)

Unit 3 [T1] [T2]

A model of The Image Degradation / Restoration Process, Noise Models, Restoration in the presence of Noise Only Spatial Filtering, Periodic Noise Reduction by Frequency Domain Filtering, Linear Position-Invariant Degradations, Estimation of Degradation Function, Inverse filtering, Wiener filtering, Constrained Least Square Filtering, Geometric Mean Filter, Geometric Transformations. (8 lectures)

Unit 4

Compression [T1]: Image Compression Coding, Interpixel and Psycho visual Redundancy, Image Compression models, Elements of Information Theory, Error free comparison, Lossy compression, Image compression standards. (6 lectures)

Image Segmentation [T1]: Detection of Discontinuities, Edge linking and boundary detection, Thresholding, Region Oriented Segmentation, Motion based segmentation.

Representation and Description [T1]: Representation, Boundary Descriptors, Regional Descriptors, Use of Principal Components for Description, Introduction to Morphology, Some basic Morphological Algorithms. Patterns and Pattern Classes, Decision-Theoretic Methods, Structural Methods (10 lectures)

Text Books:

[T1] Rafael C. Conzalez & Richard E. Woods, "Digital Image Processing", 2nd edition, Pearson Education, 2004.

[T2] A.K. Jain, "Fundamental of Digital Image Processing", PHI, 2003.

Reference Books:

[R1] Rosefield Kak, "Digital Picture Processing", 1999.

[R2] W.K. Pratt, "Digital Image Processing", 2000.

Code No: ITV-751	**L**	**P**	**C**
Lab: Based on following paper	**2**	**2**	

The experiments will be based on Algorithm for VLSI Design Automation

Code No: ITV-753	**L**	**P**	**C**
Lab: Based on Second Elective	**2**	**2**	

The experiments will be based on second elective

Code No: ITV-755	**L**	**P**	**C**
Lab: Minor Project			**10**

The student will submit a synopsis at the beginning of the semester for the approval to the school project committee in a specified format. The student will have to present the progress of the work through seminars and progress report. A report must be submitted to the school for evaluation purpose at the end of the semester in a specified format

Code No: ITV-752 **C**
Subject: Dissertation **22**

The student will submit a synopsis at the beginning of the semester for the approval from the school project committee in a specified format. Synopsis must be submitted within a two weeks. The first defense, for the dissertation work, should be held with in a one month. Dissertation Report must be submitted in a specified format to the school for evaluation purpose.

Code No: ITV-754 **C**
Subject: Seminar & Progress Report **4**

The student will have to present the progress of the dissertation work through seminars and progress reports at the interval of four weeks.